Block I
Apollo Guidance Computer (AGC)

How to build one in your basement

Part 4: Memory (MEM) Module

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December, 2004

Abstract

This report describes my successful project to build a working reproduction of the 1964 prototype for the Block I Apollo Guidance Computer. The AGC is the flight computer for the Apollo moon landings, and is the world's first integrated circuit computer.

I built it in my basement. It took me 4 years.

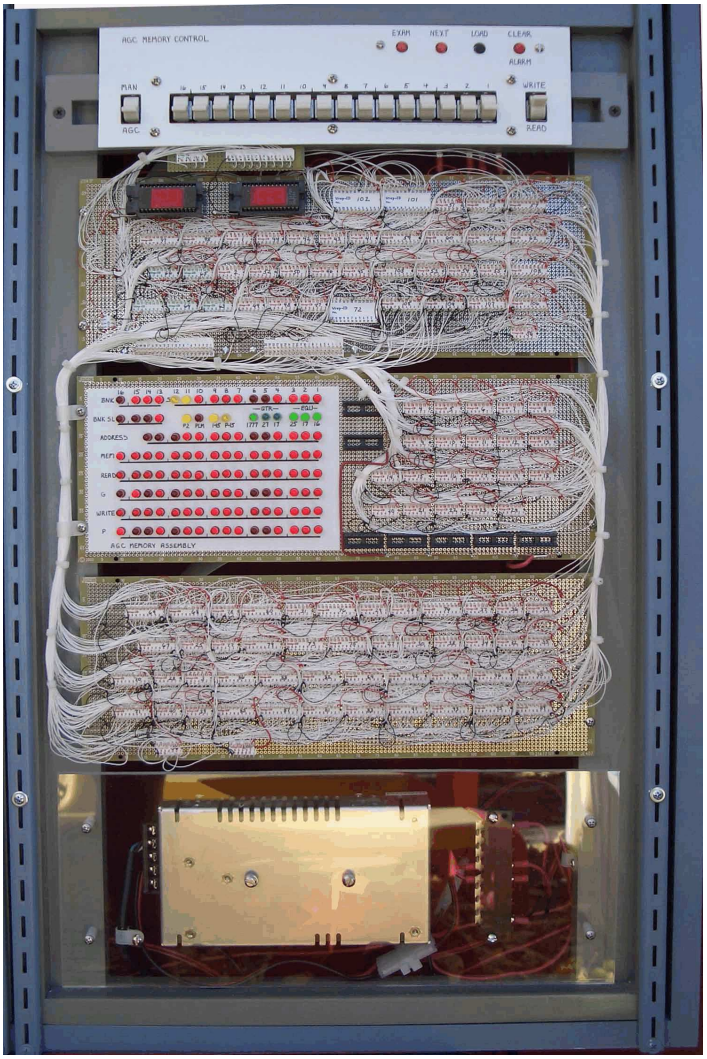
If you like, you can build one too. It will take you less time, and yours will be better than mine.

I documented my project in 9 separate .pdf files:

Part 1	Overview: Introduces the project.
Part 2	CTL Module: Design and construction of the control module.
Part 3	PROC Module: Design and construction of the processing (CPU) module.
Part 4	MEM Module: Design and construction of the memory module.
Part 5	IO Module: Design and construction of the display/keyboard (DSKY) module.
Part 6	Assembler: A cross-assembler for AGC software development.
Part 7	C++ Simulator: A low-level simulator that runs assembled AGC code.
Part 8	Flight Software: My translation of portions of the COLOSSUS 249 flight software.
Part 9	Test & Checkout: A suite of test programs in AGC assembly language.

Overview

The Memory Module (MEM) has 5 subsystems: MMI, ADR, EMM/FMM, MBF, and PAR



MMI (Memory Module external Interface)
The MMI interfaces other memory module subsystems (ADR, EMM/FMM, MBF, and PAR; described below) to external AGC modules. 40-pin IDE connectors interface to the PROC and CTL modules. Inputs from those modules are buffered to 1 LSTTL load. A 1-pin connector interfaces to the IO module.

EMM/FMM (Eraseable/Fixed Memory)
The EMM/FMM is the AGC memory. AGC memory is 16-bit words, organized into 1024 word banks. The lowest bank (bank 0) is erasable memory (EMM), originally implemented as core, but implemented here as RAM. All banks above bank 0 are fixed memory (originally implemented as rope core, but implemented here as EPROM). The Block I AGC initially had 12K words of fixed memory. This implementation has 15K.

The MSB (bit 16) in memory is an odd parity bit. The lower 15 bits hold instructions or data.

MBF (Memory Buffer Register)
The MBF has the 16-bit memory buffer register which holds 16-bit data words moving to and from memory. This is also called the G register.

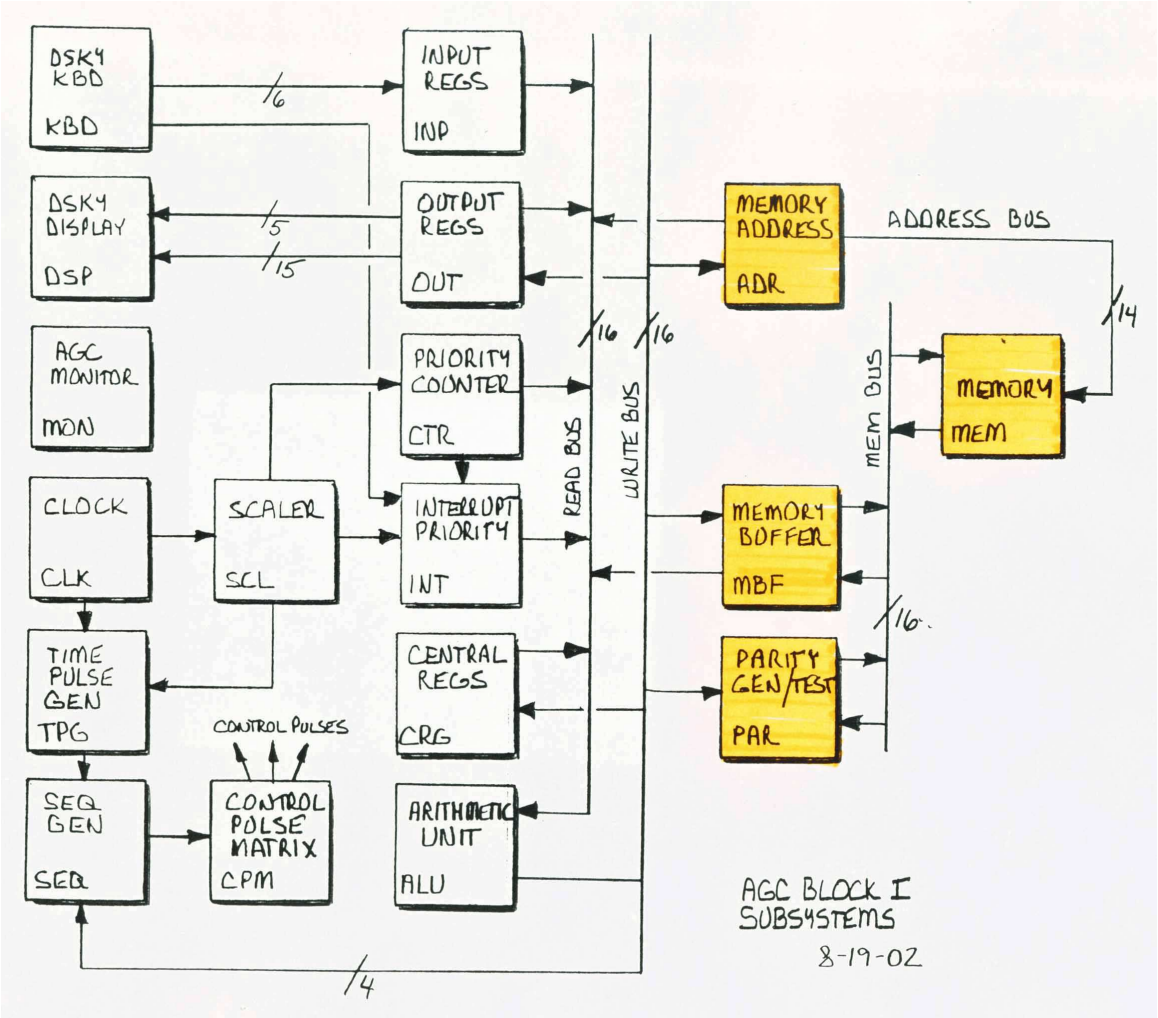
The AGC transfers data to and from memory through the G register during the "memory cycle." The memory cycle takes 12 timing pulses (11.72 microseconds). During AGC operation, data words cycle continuously from memory to the G register and then back again to memory.

There are four locations in eraseable memory, at addresses 20-23 (octal), dubbed "editing locations" because whatever was stored there would emerge shifted or rotated by one bit position. This shifting is performed in the MBF.

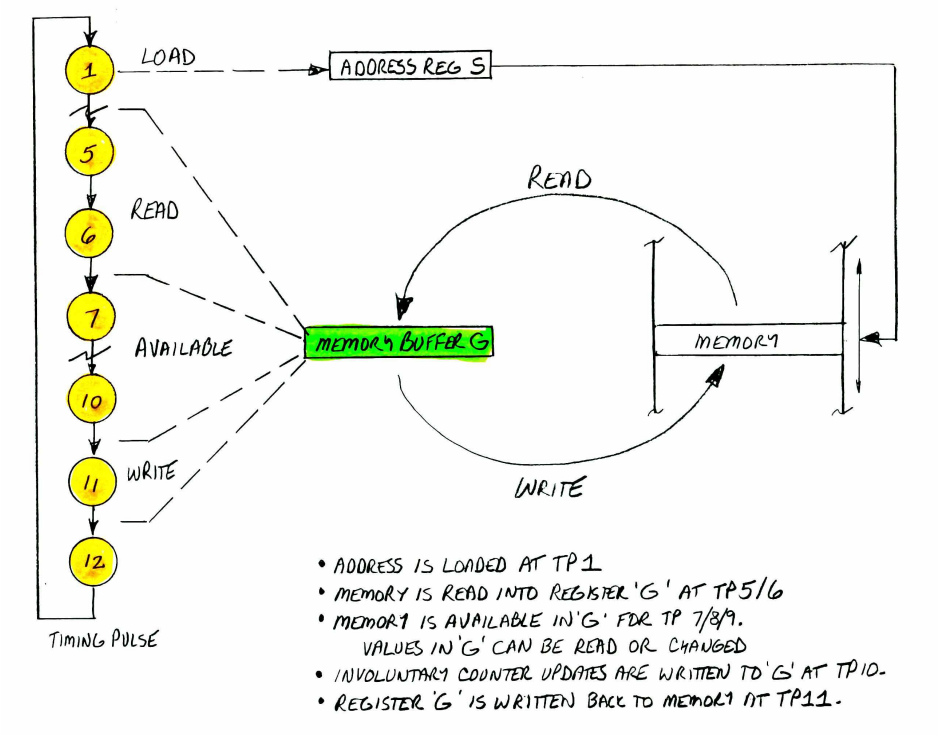
PAR (Parity Generate and Test)
The PAR generates and tests the memory parity bit. The lower 15 bits of each memory word

hold AGC instructions or data. Each word is protected by a 16th "odd parity" bit. This bit is set to 1 or 0 by a parity generator circuit so a count of the 1's in each memory word always produces an odd number. A parity checking circuit tests the parity bit during each memory cycle; if the bit doesn't match the expected value, the memory word is assumed to be corrupted and a PARITY ALARM panel light illuminates on the IO module.

ADR (Memory Address)
The ADR constructs the AGC memory address. The address is formed from the S register which holds the lower 12-bits that directly address the lowest 4K of memory, and the BANK register, which selects higher memory banks when addressing is in the fixed-switchable mode.

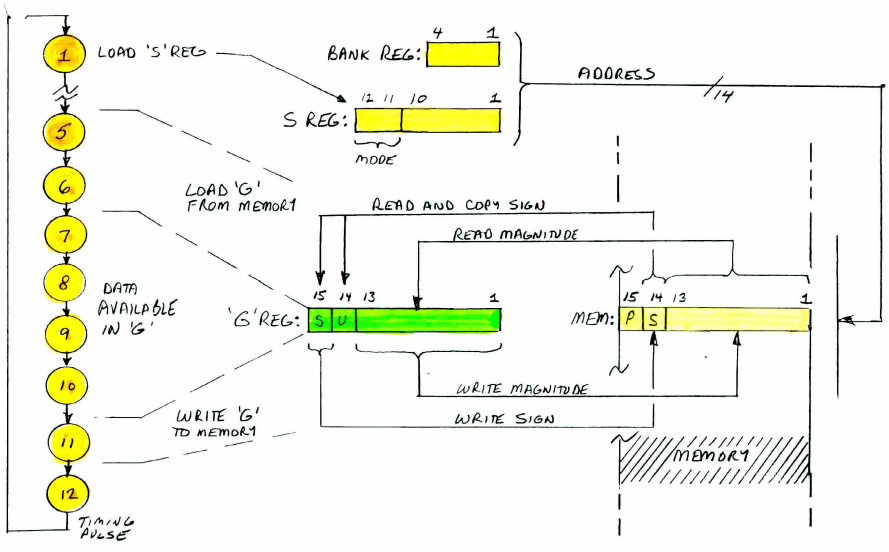


The AGC transfers data to and from memory through the G register in a process called the "memory cycle." The memory cycle takes 12 timing pulses (11.72 microseconds). The cycle begins at timing pulse 1 (TP1) when the AGC loads the memory address to be fetched into the S register in ADR. Memory hardware retrieves the data word from memory at the address specified by the S register. Words from erasable memory are deposited into the G register by timing pulse 6 (TP6); words from fixed memory are deposited by timing pulse 7. The retrieved memory word is then available in the G register for AGC access during timing pulses 7 through 10. After timing pulse 10, data in the G register is written back to memory.



The memory address is formed from the 12-bit S register and the 4-bit BANK register. Memory in the lowest 4 1K banks is directly addressed by the S register. The higher 1K banks (5-12) are address through the bank register as described in the ADR subsystem section of this document.

The high-order bit in memory (bit 15) is an odd parity bit. If the memory word is a data word, the 14th bit is the sign, and bits 13 through 1 hold the magnitude. The number representation is 1's complement.



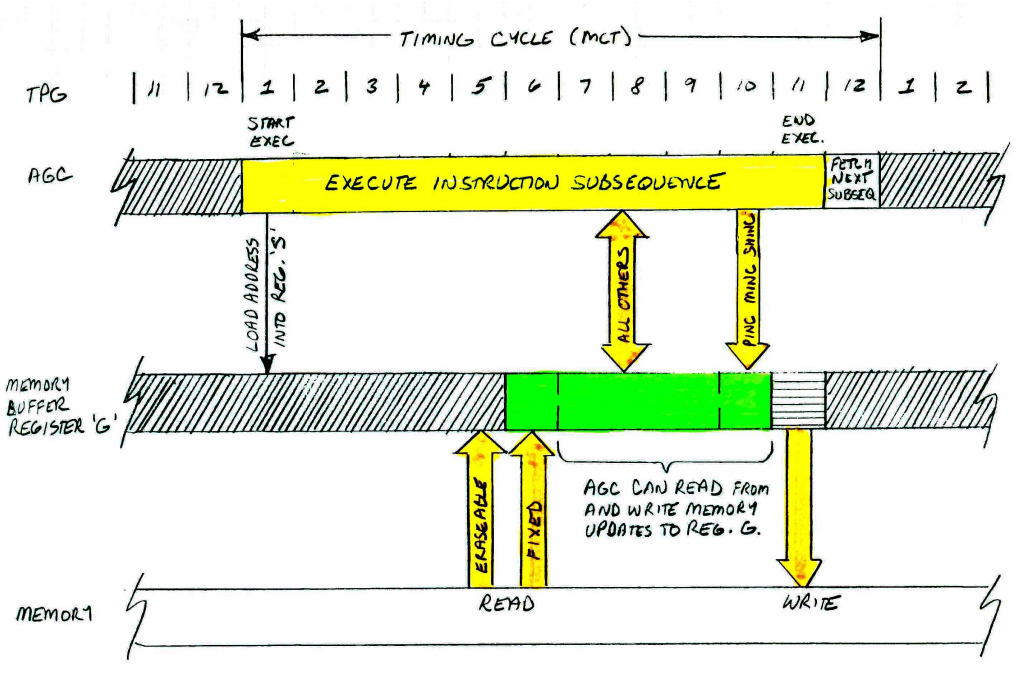
The first half of the memory cycle copies data from memory to the G register, The sign bit in memory (bit 14) is copied to bits 15 and 14 of the G register. Bits 13 through 1 in memory are

copied to bits 13 through 1 in G. This is performed in the MBF and EMM/FMM subsystems. The parity bit (bit 16 in memory) is read by the PAR subsystem and tested against parity generated on the memory word copied into G. If the parity bits fail to match, a parity alarm is generated.

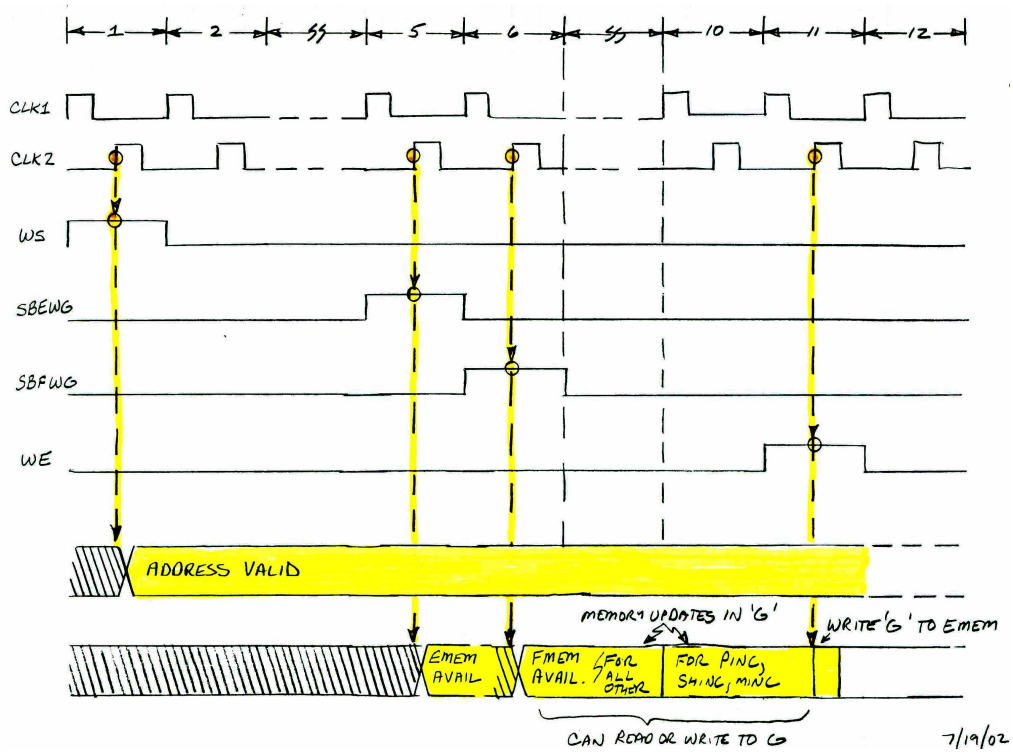
The 14th bit in the G register (and the central registers in the AGC) is called the Uncorrected Sign (US). This extra sign bit is used as an overflow indication in multi-word operations. Normally, the Sign and Uncorrected sign should agree. When overflow or underflow conditions occur, both signs will disagree, and are reconciled by software in an operation at the end of a long string of multi-word computations.

At the end of the memory cycle, the G register is copied back to memory. The sign bit in G (bit 15) is written to the sign bit (bit 14) in memory. Bits 13 through 1 in G are written to bits 13 through 1 in memory. A new odd parity bit is computed in the PAR subsystem and written to the 16th bit in memory.

These diagrams show the timing of the memory cycle. The top chart is a little more conceptual; the bottom chart shows the clock cycles and control pulses directly associated with reading eraseable memory (SBEWG) or fixed memory (SBFWG) to the G register (the 'WG' part means 'write to G'). The WE pulse writes G back to memory.



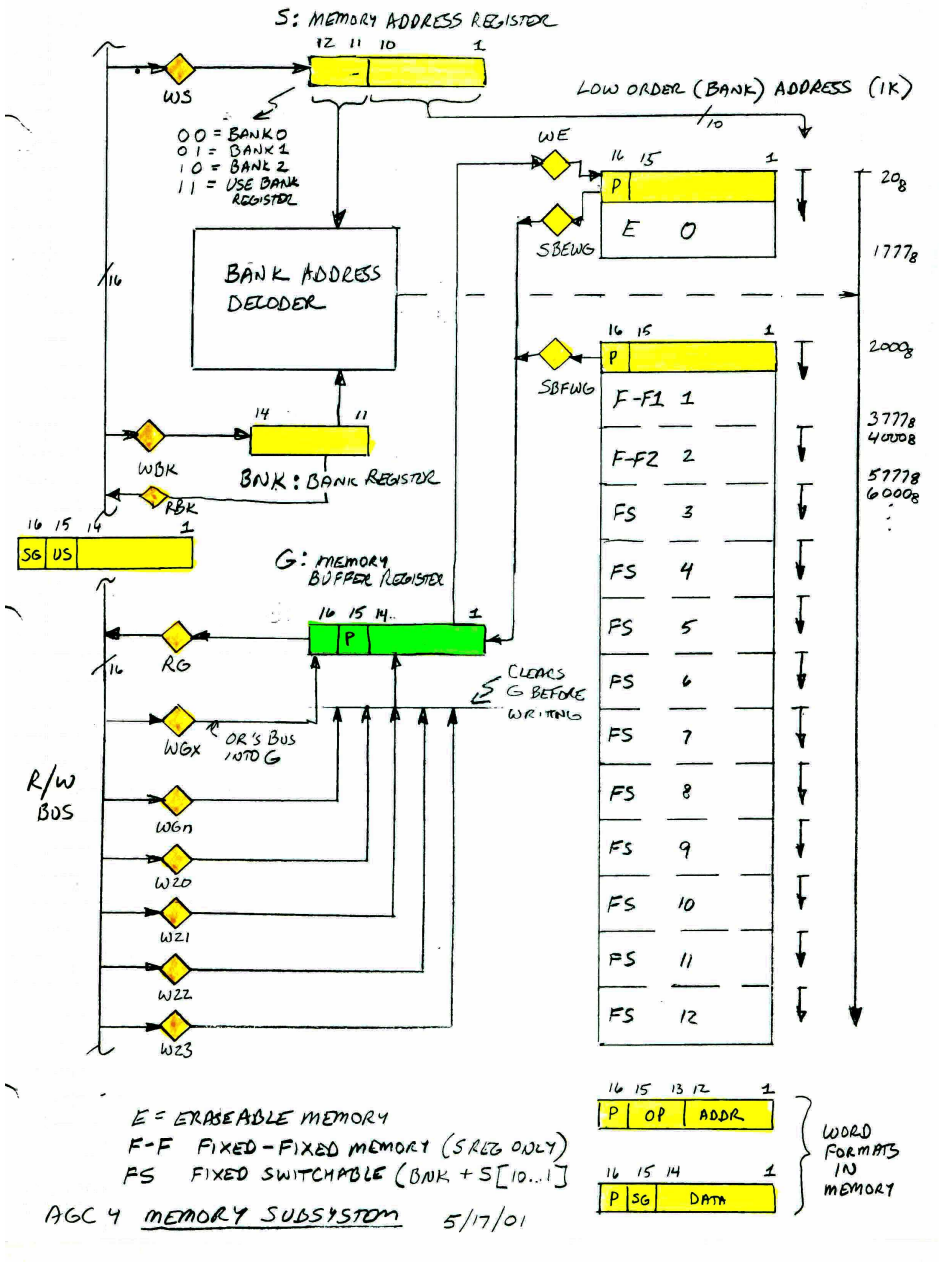
CLK1 steps the sequencer in the CTL module that enables the control signals. The signals have time to settle between CLK1 and CLK2. Data transfer occurs on CLK2.



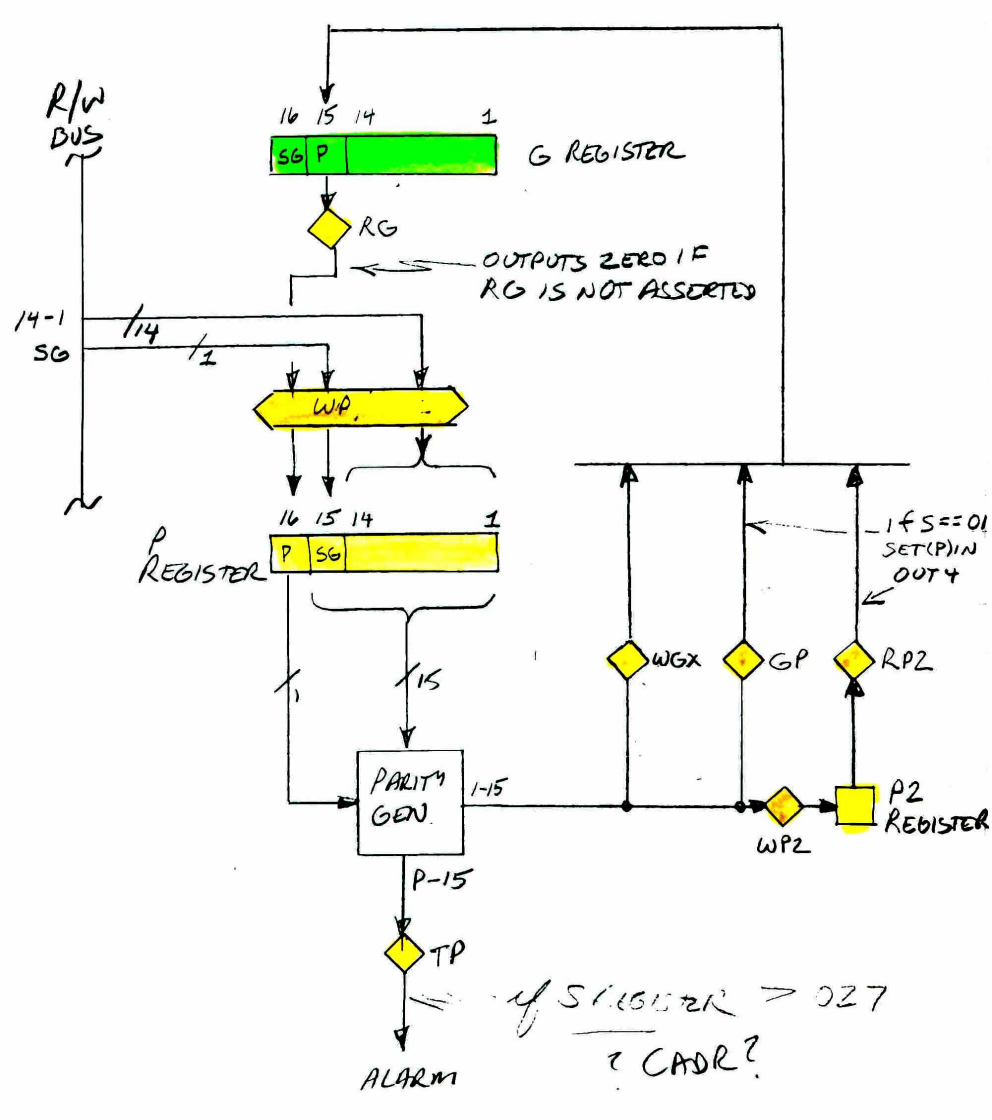
This is a functional diagram of the ADR, EMM/FMM, and MBF subsystems in the MEM module.

The diagram is mine, but the style is borrowed from original AGC documentation: control signals are represented by diamonds. The arrows show the direction of data flow. When a control signal is asserted, data is allowed to flow through the diamond.
For example, when WE is asserted, the contents of the G register are written into eraseable memory (bank 0).

Note the different formats for data and instruction word in memory, shown at the bottom of the diagram.

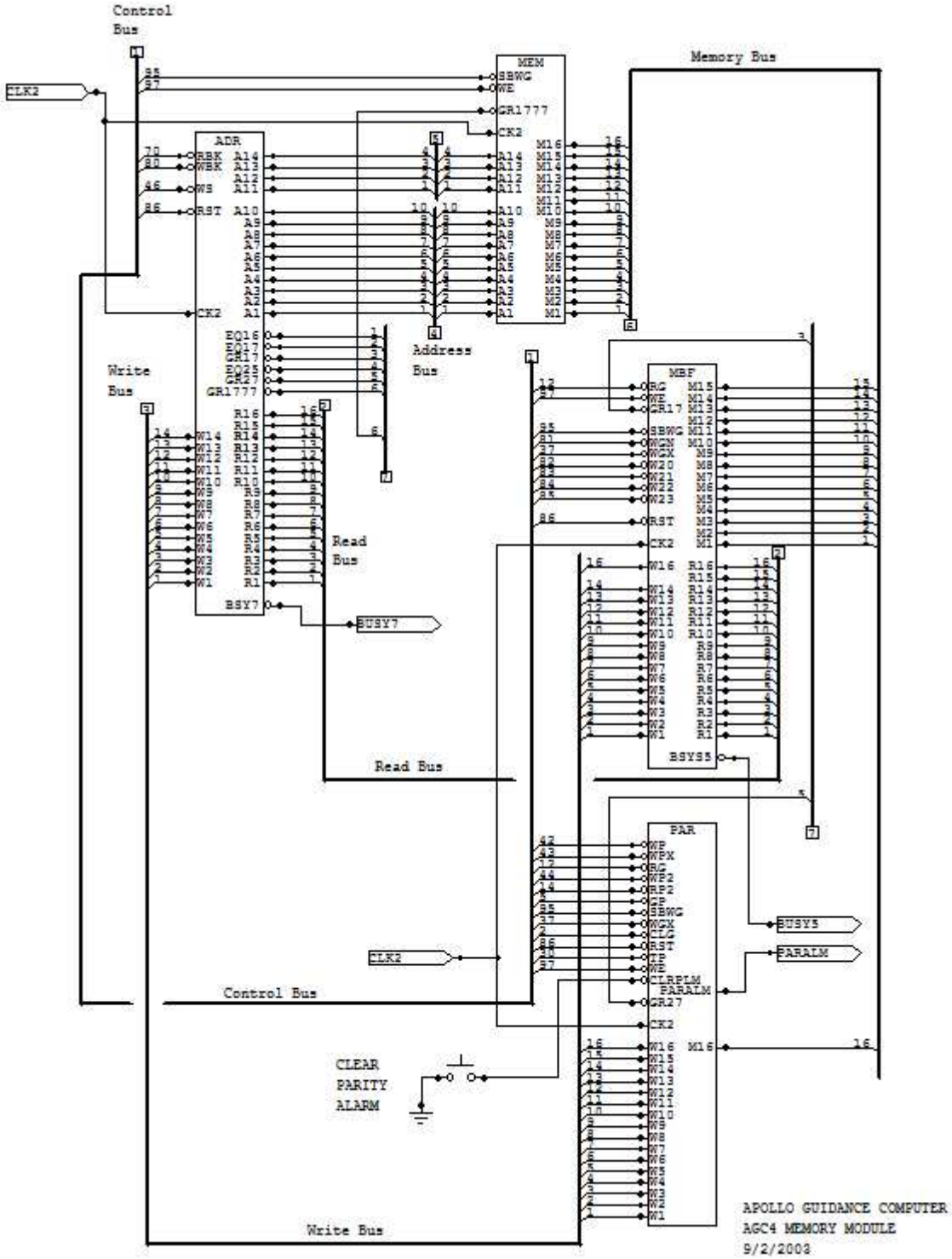


This is a functional diagram of the PAR subsystem in the MEM module. The diagram was developed during the early stages of my AGC architecture analysis in 2001.



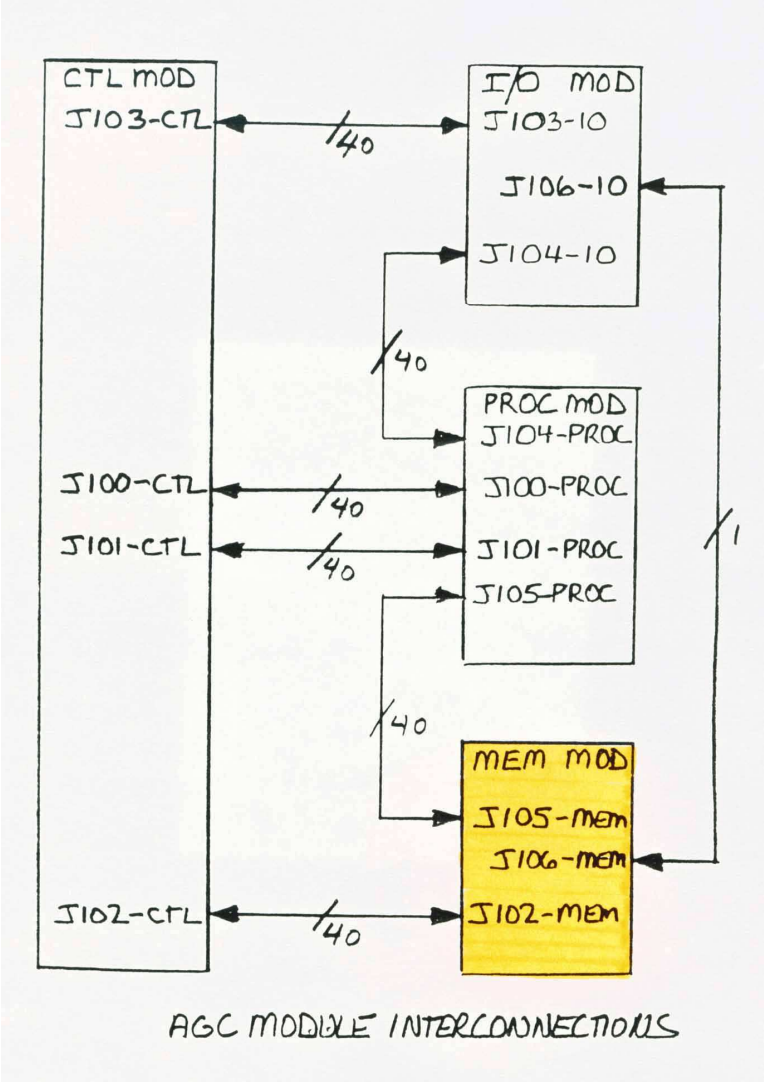
MEM Internal Subsystem Interconnections

This diagram shows internal interconnections for subsystems in the MEM module.



MEM Module External Interfaces

The MEM module interfaces to the PROC and CTL modules through 40-pin IDE ribbon cables.



J102-CTL: CTL-to-MEM I/F
J102 is a 40-pin IDE cable that connects the MEM module to the CTL module.

INPUTS (to CTL):

PIN	signal	full name	state definition
1	WE	WRITE EMEM (97)	0=Write E-MEM from G
2	SBWG	WRITE G (95)	0=Write G from memory
3	GENRST	GENERAL RESET (86)	0=General Reset
4	W23	WRITE ADDR 23 (85)	0=Write into SL
5	W22	WRITE ADDR 22 (84)	0=Write into CYL
6	W21	WRITE ADDR 21 (83)	0=Write into SR
7	W20	WRITE ADDR 20 (82)	0=Write into CYR
8	WGn	WRITE G NORMAL (81)	0=Write G (normal gates)
9	WBK	WRITE BNK (80)	0=Write BNK reg
10	RBK	READ BNK (70)	0=Read BNK reg
11	WS	WRITE S (46)	0=Write S
12	WP2	WRITE P2 (44)	0=Write P2
13	WPx	WRITE P NO RESET (43)	0=Write P (do not reset)
14	WP	WRITE P (42)	0=Write P
15	WGx	WRITE G NO RESET (37)	0=Write G (do not reset)
16	TP	TEST PARITY (30)	0=Test parity
17	RP2	READ PARITY 2 (14)	0=Read parity 2
18	RG	READ G (12)	0=Read G
19	GP	GEN PARITY (5)	0=Generate Parity
20	CLG	CLR G (2)	0=Clear G
21	CLK2	CLOCK2	1.024 MHz AGC clock phase 2 (normally low)
22	CLK1	CLOCK1	1.024 MHz AGC clock phase 2 (normally low)
23	NPURST	POWER UP RESET	0=reset, 1=normal operation.
24	SWCLK	DEBOUNCE CLOCK	low freq clk for switch debounce (not used)
25	FCLK	CLOCK MODE	1=free-running clk mode; 0=single clk mode

OUTPUTS (from CTL):

PIN	signal	full name	state definition
31	EQU_16	ADDRESS = 016 (1)	0=CADR in register S = 016
32	EQU_17	ADDRESS = 017 (2)	0=CADR in register S= 017
33	GTR_17	ADDRESS > 017 (3)	0=CADR in register S > 017
34	EQU_25	ADDRESS = 025 (4)	0=CADR in register S = 025
35	GTR_27	ADDRESS > 027 (5)	0=CADR in register S > 027
36	GTR_1777	ADDRESS > 01777 (6)	0=CADR in register S > 01777
37	AD_1	ADDRESS (1)	where AD_4 is MSB, AD_1 is LSB
38	AD_2	ADDRESS (2)	
39	AD_3	ADDRESS (3)	
40	AD_4	ADDRESS (4)	

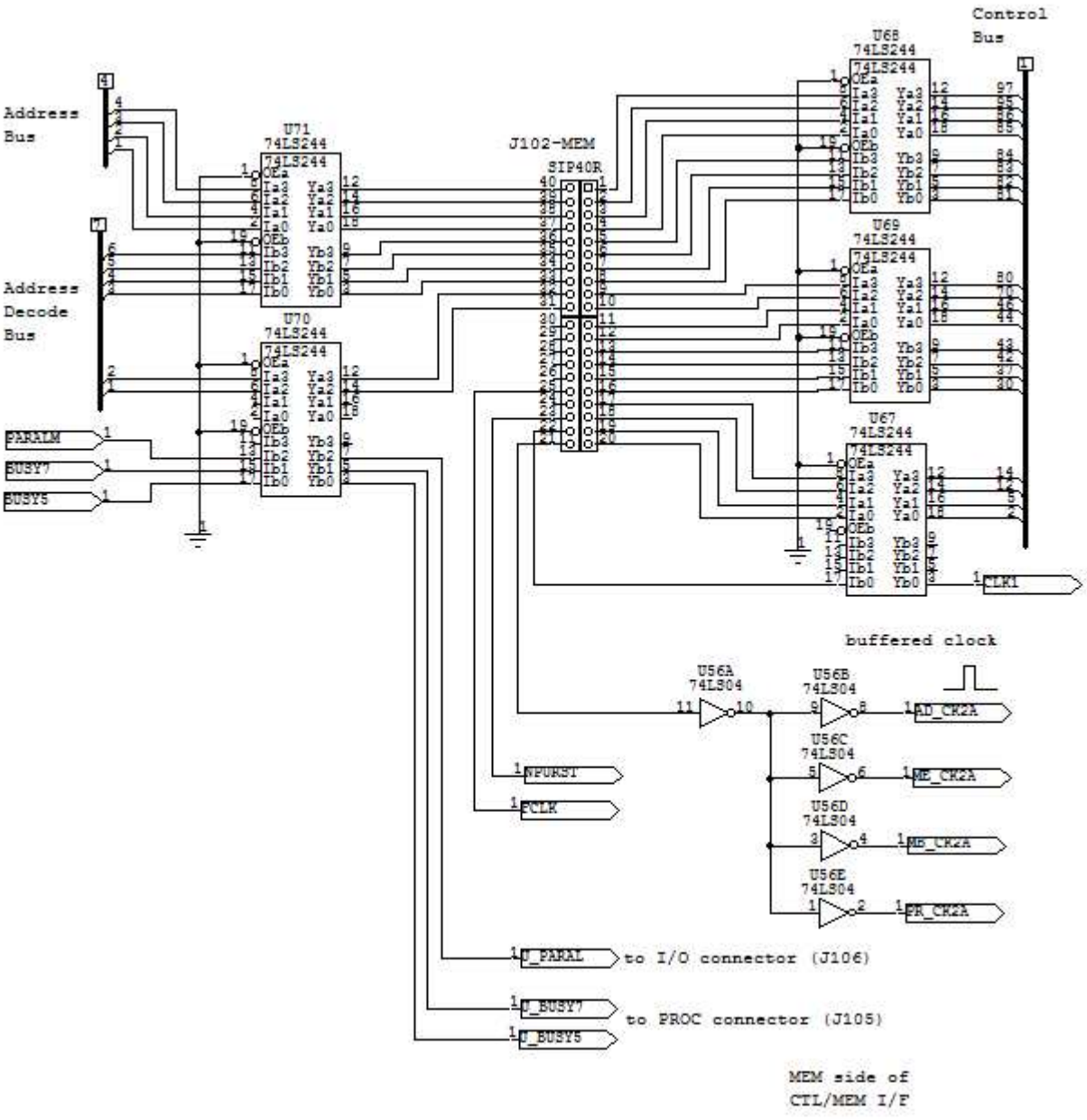
J105-MEM: MEM-to-PROC I/F
J102 is a 40-pin IDE cable that connects the MEM module to the PROC module.

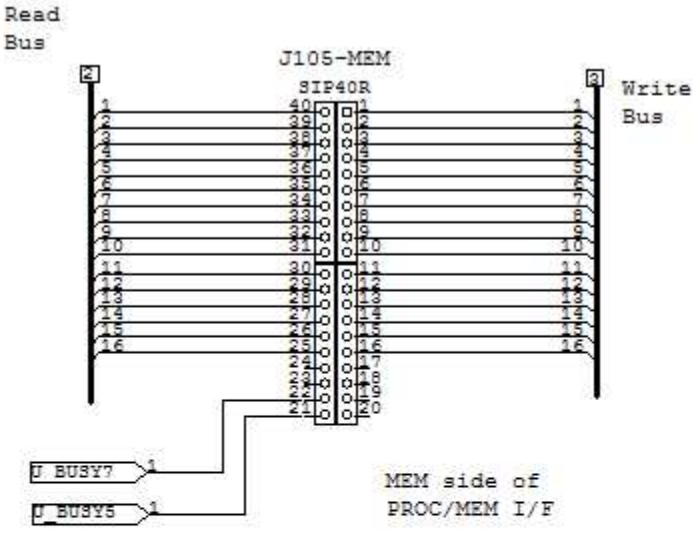
INPUTS (to MEM):

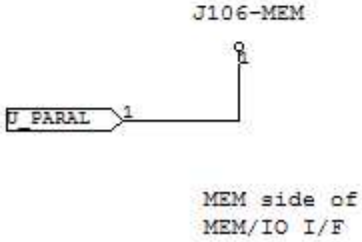
PIN	signal	full name	state definition
1	WB_01	WRITE BUS 01	(lsb)
2	WB_02	WRITE BUS 02	
3	WB_03	WRITE BUS 03	
4	WB_04	WRITE BUS 04	
5	WB_05	WRITE BUS 05	
6	WB_06	WRITE BUS 06	
7	WB_07	WRITE BUS 07	
8	WB_08	WRITE BUS 08	
9	WB_09	WRITE BUS 09	
10	WB_10	WRITE BUS 10	
11	WB_11	WRITE BUS 11	
12	WB_12	WRITE BUS 12	
13	WB_13	WRITE BUS 13	
14	WB_14	WRITE BUS 14	
15	WB_15	WRITE BUS 15	US (overflow) bit
16	WB_16	WRITE BUS 16	SG (sign) bit

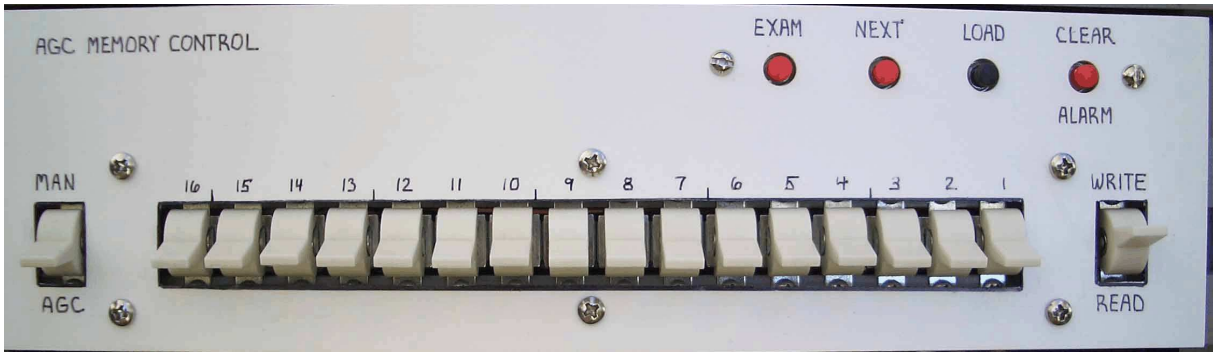
OUTPUTS (from MEM):

PIN	signal	full name	state definition
40	RB_01	READ BUS 01	(lsb)
39	RB_02	READ BUS 02	
38	RB_03	READ BUS 03	
37	RB_04	READ BUS 04	
36	RB_05	READ BUS 05	
35	RB_06	READ BUS 06	
34	RB_07	READ BUS 07	
33	RB_08	READ BUS 08	
32	RB_09	READ BUS 09	
31	RB_10	READ BUS 10	
30	RB_11	READ BUS 11	
29	RB_12	READ BUS 12	
28	RB_13	READ BUS 13	
27	RB_14	READ BUS 14	
26	RB_15	READ BUS 15	US (overflow) bit
25	RB_16	READ BUS 16	SG (sign) bit
22	BUSY7	READ BUS BUSY	0=BNK register output to read bus
21	BUSY5	READ BUS BUSY	0=G register output to read bus


Control
Bus
Address
Bus
Address
Decode
Bus
U71
74LS244
U70
74LS244
J102-MEM
SIP40R
U68
74LS244
U69
74LS244
U67
74LS244
PARALM
BUSY7
BUSY5
CLK1
buffered clock
U56A
74LS04
U56B
74LS04
U56C
74LS04
U56D
74LS04
U56E
74LS04
AD_CK2A
ME_CK2A
MB_CK2A
PR_CK2A
NPURST
PCLK
O_PARAL
to I/O connector (J106)
O_BUSY7
to PROC connector (J105)
O_BUSY5
MEM side of
CTL/MEM I/F


Read
Bus
J105-MEM
SIP40R
Write
Bus
U_BUSY7
U_BUSY5
MEM side of
PROC/MEM I/F


J106-MEM
U_PARAL
MEM side of
MEM/IO I/F



MEM CONTROL PANEL SWITCHES

AGC/MANUAL	Permits memory to be examined and loaded when the switch is in the MANUAL position and the AGC is halted.
EXAM	Loads the address counter with the contents of the switch register. To work, the following switches must also be set: AGC/MANUAL --> MANUAL
NEXT	Steps the address to the next location. To work, the following switches must also be set: AGC/MANUAL --> MANUAL
READ/WRITE	Displays memory contents in the READ position; displays switch register contents in the WRITE position.
LOAD	Load memory with data manually entered into the switch register. To work, the following switches must also be set prior to LOAD: CLOCK CONTROL (on CTL module) --> STEP; AGC/MANUAL --> MANUAL; READ/WRITE --> WRITE
CLEAR PARITY	Clears a parity alarm indication by resetting the parity alarm (PALM) register. The parity alarm indicator is on the IO module.

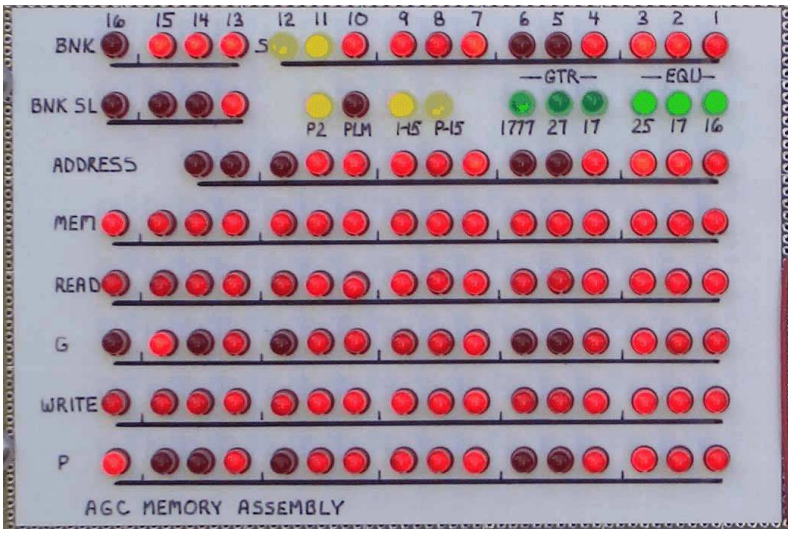
MEM CONTROL SWITCH CONNECTIONS

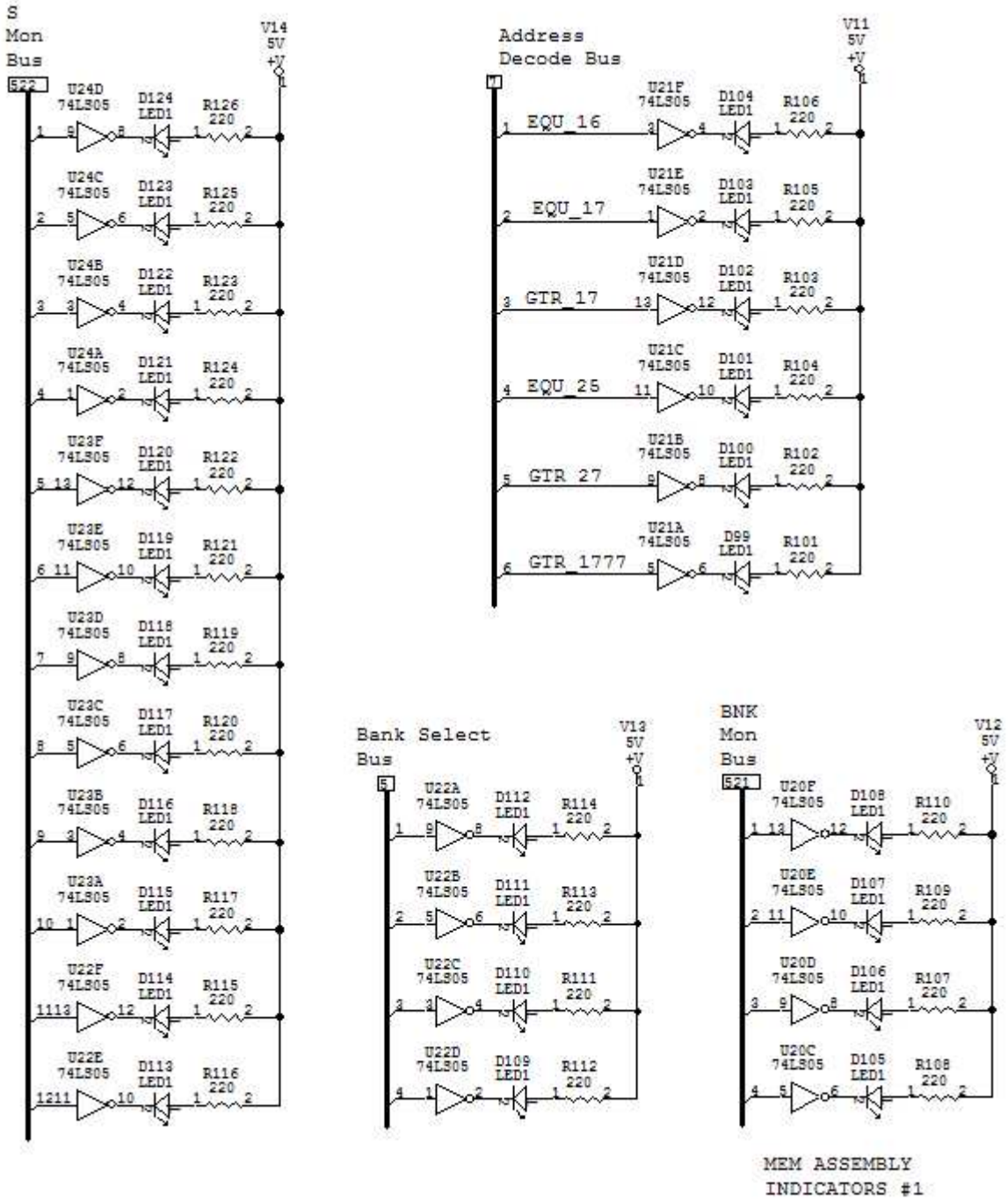
PIN	signal	state definition
1	READ/WRITE	GND = read
2	AGC/MANUAL	GND = manual
3	EXAM	GND = examine
4	NEXT	GND = examine next
5	CLEAR PARITY	GND = clear
6	LOAD	LOAD switch contact
7	LOAD	LOAD switch contact

PIN	signal	full name	state definition
1	D1	DATA1	LSB on switch bus 101
2	D2	DATA2	
3	D3	DATA3	
4	D4	DATA4	
5	D5	DATA5	
6	D6	DATA6	
7	D7	DATA7	
8	D8	DATA8	
9	D9	DATA9	
10	D10	DATA10	
11	D11	DATA11	
12	D12	DATA12	
13	D13	DATA13	
14	D14	DATA14	
15	D15	DATA15	
16	D16	DATA16	LSB on switch bus 101
17	GND	GND	

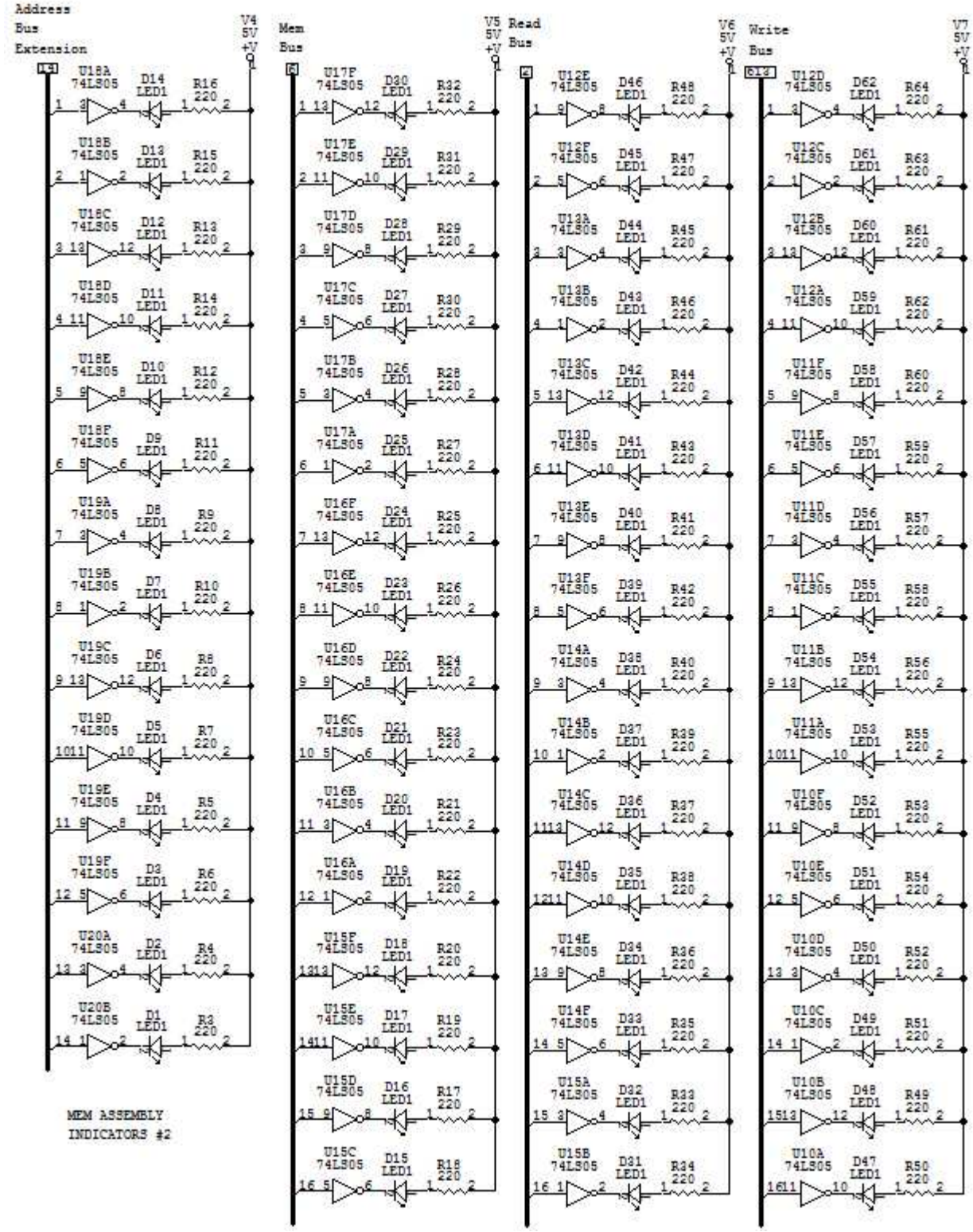
MEM INDICATORS

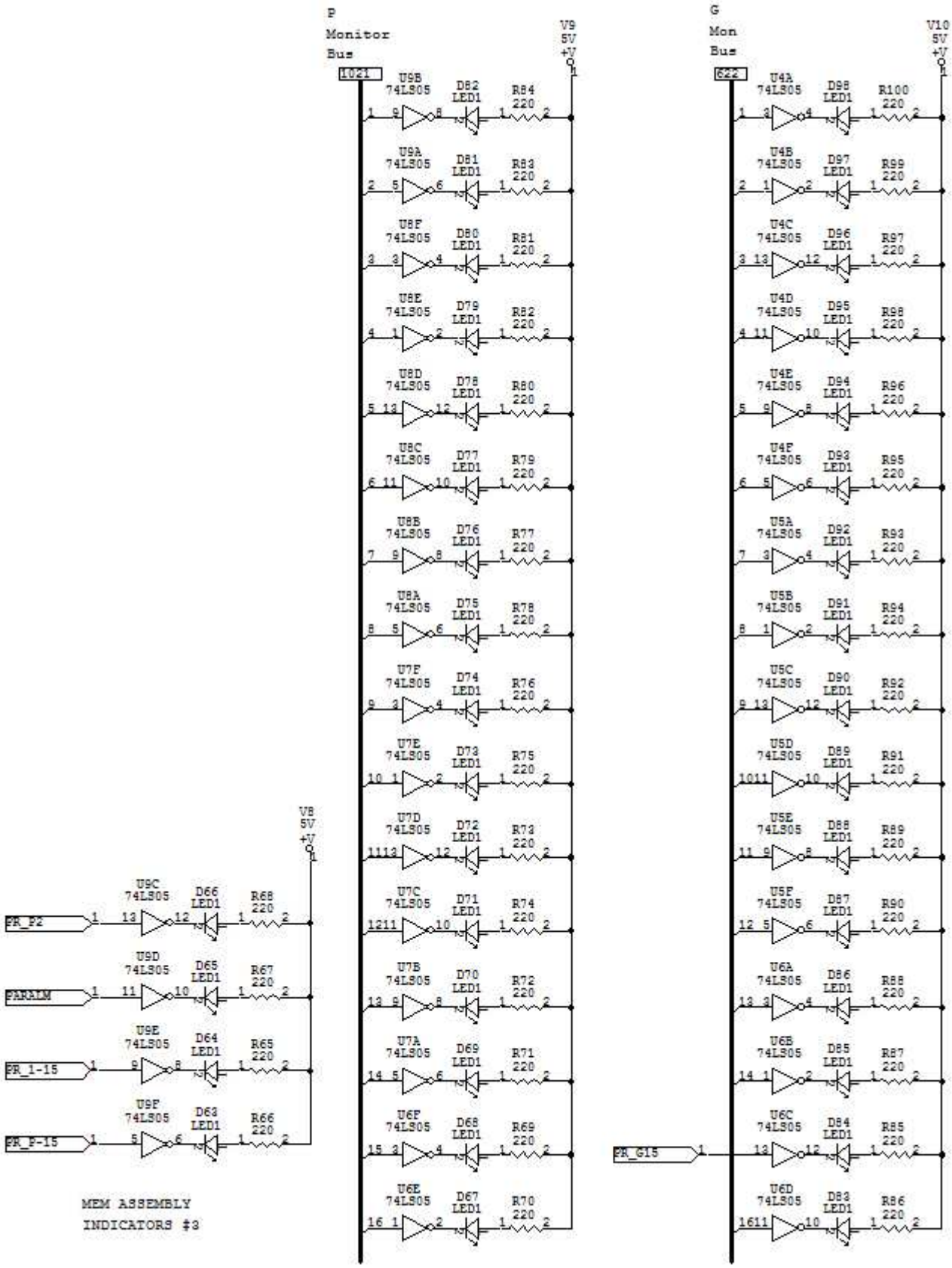
These indicator lamps show the current state of all registers and some additional, important logic signals produced by the MEM module. AGC numbers are represented in octal, so all register lamps are in groups of three. At the time the photo was taken the AGC was running the COLOSSUS 249 flight software load, executing Verb 16, Noun 36: a monitor verb which displays the AGC real time clock.





MEM ASSEMBLY
INDICATORS #1


Address
Bus
Extension
Mem
Bus
Read
Bus
Write
Bus
V4
5V
+V
V5
5V
+V
V6
5V
+V
V7
5V
+V
U18A 74LS05 D14 LED1 R16 220
U18B 74LS05 D13 LED1 R15 220
U18C 74LS05 D12 LED1 R13 220
U18D 74LS05 D11 LED1 R14 220
U18E 74LS05 D10 LED1 R12 220
U18F 74LS05 D9 LED1 R11 220
U19A 74LS05 D8 LED1 R9 220
U19B 74LS05 D7 LED1 R10 220
U19C 74LS05 D6 LED1 R8 220
U19D 74LS05 D5 LED1 R7 220
U19E 74LS05 D4 LED1 R5 220
U19F 74LS05 D3 LED1 R6 220
U20A 74LS05 D2 LED1 R4 220
U20B 74LS05 D1 LED1 R3 220
U17F 74LS05 D30 LED1 R32 220
U17E 74LS05 D29 LED1 R31 220
U17D 74LS05 D28 LED1 R29 220
U17C 74LS05 D27 LED1 R30 220
U17B 74LS05 D26 LED1 R28 220
U17A 74LS05 D25 LED1 R27 220
U16F 74LS05 D24 LED1 R25 220
U16E 74LS05 D23 LED1 R26 220
U16D 74LS05 D22 LED1 R24 220
U16C 74LS05 D21 LED1 R23 220
U16B 74LS05 D20 LED1 R21 220
U16A 74LS05 D19 LED1 R22 220
U15F 74LS05 D18 LED1 R20 220
U15E 74LS05 D17 LED1 R19 220
U15D 74LS05 D16 LED1 R17 220
U15C 74LS05 D15 LED1 R18 220
U12E 74LS05 D46 LED1 R48 220
U12F 74LS05 D45 LED1 R47 220
U13A 74LS05 D44 LED1 R45 220
U13B 74LS05 D43 LED1 R46 220
U13C 74LS05 D42 LED1 R44 220
U13D 74LS05 D41 LED1 R43 220
U13E 74LS05 D40 LED1 R41 220
U13F 74LS05 D39 LED1 R42 220
U14A 74LS05 D38 LED1 R40 220
U14B 74LS05 D37 LED1 R39 220
U14C 74LS05 D36 LED1 R37 220
U14D 74LS05 D35 LED1 R38 220
U14E 74LS05 D34 LED1 R36 220
U14F 74LS05 D33 LED1 R35 220
U15A 74LS05 D32 LED1 R33 220
U15B 74LS05 D31 LED1 R34 220
U12D 74LS05 D62 LED1 R64 220
U12C 74LS05 D61 LED1 R63 220
U12B 74LS05 D60 LED1 R61 220
U12A 74LS05 D59 LED1 R62 220
U11F 74LS05 D58 LED1 R60 220
U11E 74LS05 D57 LED1 R59 220
U11D 74LS05 D56 LED1 R57 220
U11C 74LS05 D55 LED1 R58 220
U11B 74LS05 D54 LED1 R56 220
U11A 74LS05 D53 LED1 R55 220
U10F 74LS05 D52 LED1 R53 220
U10E 74LS05 D51 LED1 R54 220
U10D 74LS05 D50 LED1 R52 220
U10C 74LS05 D49 LED1 R51 220
U10B 74LS05 D48 LED1 R49 220
U10A 74LS05 D47 LED1 R50 220
MEM ASSEMBLY
INDICATORS #2


P
Monitor
Bus
1021
V9
5V
+V
U9B 74LS05 D82 LED1 R84 220
U9A 74LS05 D81 LED1 R83 220
U8F 74LS05 D80 LED1 R81 220
U8E 74LS05 D79 LED1 R82 220
U8D 74LS05 D78 LED1 R80 220
U8C 74LS05 D77 LED1 R79 220
U8B 74LS05 D76 LED1 R77 220
U8A 74LS05 D75 LED1 R78 220
U7F 74LS05 D74 LED1 R76 220
U7E 74LS05 D73 LED1 R75 220
U7D 74LS05 D72 LED1 R73 220
U7C 74LS05 D71 LED1 R74 220
U7B 74LS05 D70 LED1 R72 220
U7A 74LS05 D69 LED1 R71 220
U6F 74LS05 D68 LED1 R69 220
U6E 74LS05 D67 LED1 R70 220
G
Mon
Bus
622
V10
5V
+V
U4A 74LS05 D98 LED1 R100 220
U4B 74LS05 D97 LED1 R99 220
U4C 74LS05 D96 LED1 R97 220
U4D 74LS05 D95 LED1 R98 220
U4E 74LS05 D94 LED1 R96 220
U4F 74LS05 D93 LED1 R95 220
U5A 74LS05 D92 LED1 R93 220
U5B 74LS05 D91 LED1 R94 220
U5C 74LS05 D90 LED1 R92 220
U5D 74LS05 D89 LED1 R91 220
U5E 74LS05 D88 LED1 R89 220
U5F 74LS05 D87 LED1 R90 220
U6A 74LS05 D86 LED1 R88 220
U6B 74LS05 D85 LED1 R87 220
U6C 74LS05 D84 LED1 R85 220
U6D 74LS05 D83 LED1 R86 220
PR_G15
V8
5V
+V
U9C 74LS05 D66 LED1 R68 220
U9D 74LS05 D65 LED1 R67 220
U9E 74LS05 D64 LED1 R65 220
U9F 74LS05 D63 LED1 R66 220
PR_P2
PARALM
PR_1-15
PR_P-15
MEM ASSEMBLY
INDICATORS #3

ADR (Memory Address)

The AGC has a 14-bit address range. Memory address is selected by the 12-bit S register and the 4-bit BANK register.

- S: the 12-bit memory address register, which holds the lower portion of the memory address.
- BANK: the 4-bit memory bank register, which selects the memory bank when addressing is in the fixed-switchable mode.

Each AGC instruction has a 12-bit address field. The lower bits (1-10) address memory inside each bank. Bits 11 and 12 select the bank:

- 00: selects the erasable memory bank; the BANK register is ignored.
- 01: selects the lowest bank (bank 1) of fixed memory; the BANK register is ignored.
- 10: selects the next bank (bank 2) of fixed memory; the BANK register is ignored.
- 11: selects the BANK register, which is used to address any bank above 2. If the BANK register contains 0, 1, or 2, the BANK register is overridden and bank 3 is selected.

Banks 1 and 2 are called "fixed-fixed" memory, because they are always available, regardless of the contents of the BANK register. Banks 3 and above are called "fixed-switchable" because the selected bank is determined by the BANK register.

Type:

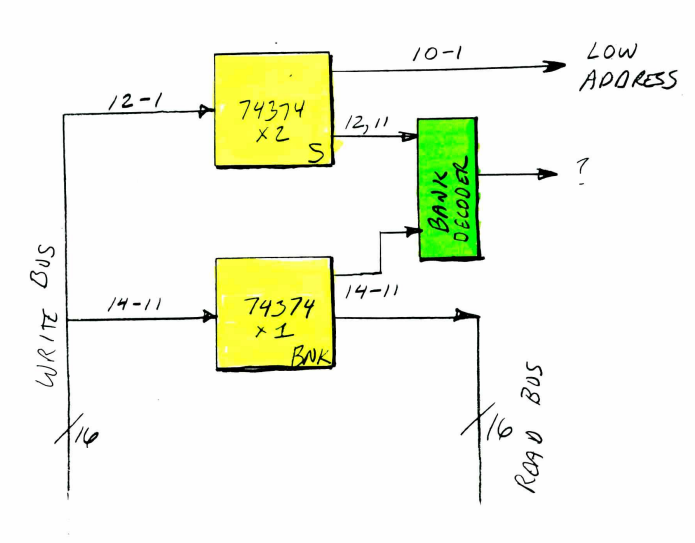
E	Eraseable Memory
FF	Fixed-Fixed Memory
FS	Fixed-Switchable Memory

14-bit address	bank	BANK type	Reg.	S Register: bits 12,11	12-bit address
00000 - 01777	0	(E)	ignored	00	0000 - 1777
02000 - 03777	1	(FF)	ignored	01	2000 - 3777
04000 - 05777	2	(FF)	ignored	10	4000 - 5777
06000 - 07777	3	(FS)	0000 - 0011	11	6000 - 7777
10000 - 11777	4	(FS)	0100	11	6000 - 7777
12000 - 13777	5	(FS)	0101	11	6000 - 7777
14000 - 15777	6	(FS)	0110	11	6000 - 7777
16000 - 17777	7	(FS)	0111	11	6000 - 7777
20000 - 21777	8	(FS)	1000	11	6000 - 7777
22000 - 23777	9	(FS)	1001	11	6000 - 7777
24000 - 25777	10	(FS)	1010	11	6000 - 7777
26000 - 27777	11	(FS)	1011	11	6000 - 7777
30000 - 31777	12	(FS)	1100	11	6000 - 7777

BANK register (B)				+ S register (S)		Decodes to address:			
B4	B3	B2	B1	S12	S11	A14	A13	A12	A11
X	X	X	X	0	0	0	0	0	0
X	X	X	X	0	1	0	0	0	1

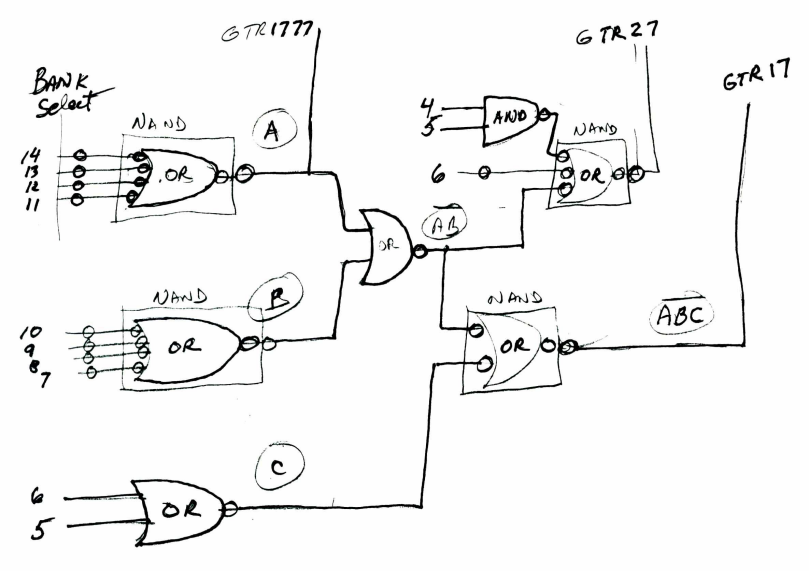
X	X	X	X	1	0	0	0	1	0
0	0	0	0	1	1	0	0	1	1
0	0	0	1	1	1	0	0	1	1
0	0	1	0	1	1	0	0	1	1
0	0	1	1	1	1	0	0	1	1
0	1	0	0	1	1	0	1	0	0
0	1	0	1	1	1	0	1	0	1
0	1	1	0	1	1	0	1	1	0
0	1	1	1	1	1	0	1	1	1
1	0	0	0	1	1	1	0	0	0
1	0	0	1	1	1	1	0	0	1
1	0	1	0	1	1	1	0	1	0
1	0	1	1	1	1	1	0	1	1
1	1	0	0	1	1	1	1	0	0
1	1	0	1	1	1	1	1	0	1
1	1	1	0	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1

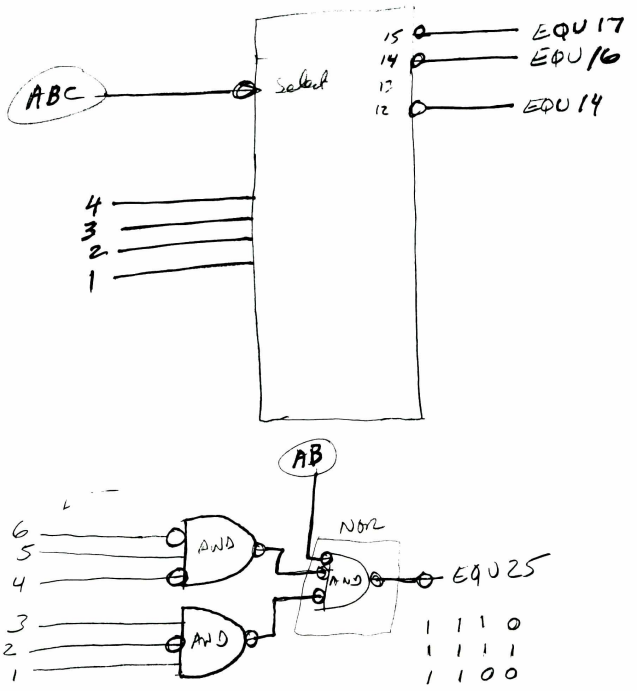
X = don't care



This is an early conceptual diagram of ADR architecture. The WRITE bus loads the BNK register or S register. Outputs from both registers feed into the bank decoder to generate the bank address.

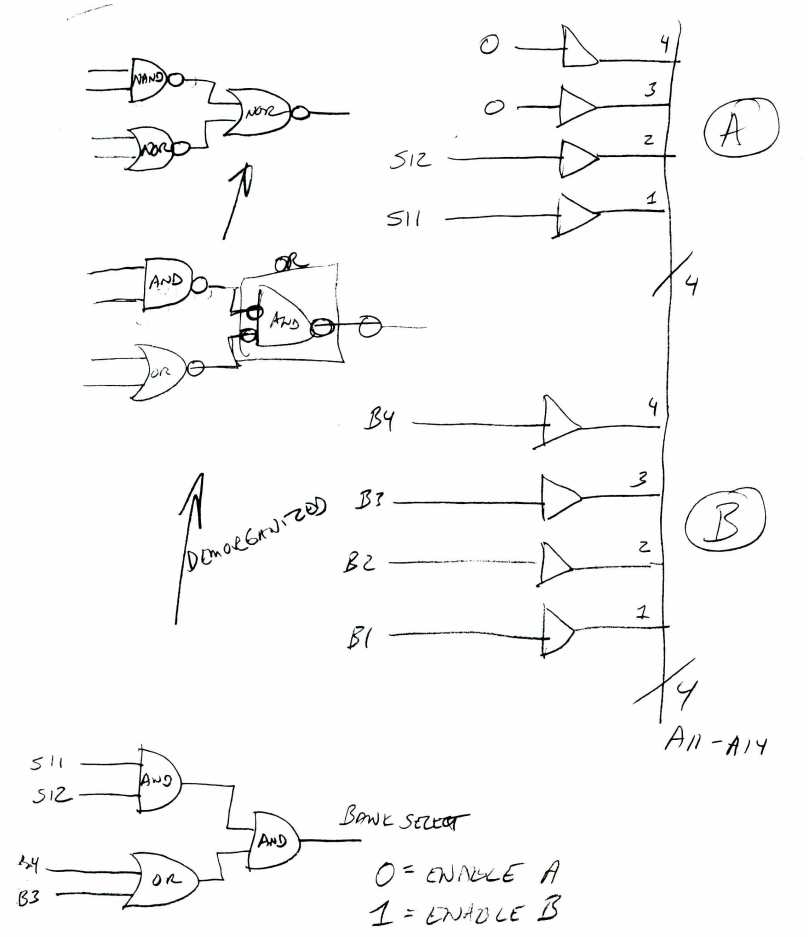
The ADR generates some logic signals to test the address. These are internally used in MEM and also made available to the external modules. The GTR signals test whether the generated address is greater than 1777, 27, or 17 (all octal).





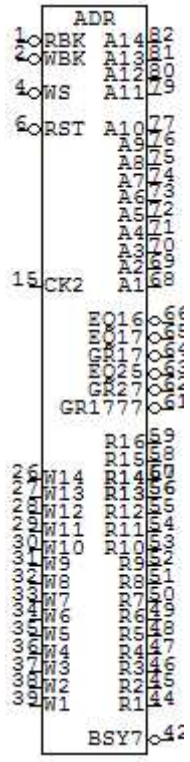
The EQU logic tests whether the generated address is equal to a specific value: 14, 16, 17, or 25.

The bank select logic chooses between the S register or a combination of the S register and the bank register to generate address bits 14-11. It uses S register bits 11 and 12 to make the decision. The selection signal enables tri-state buffer A or B to produce the correct bank address.



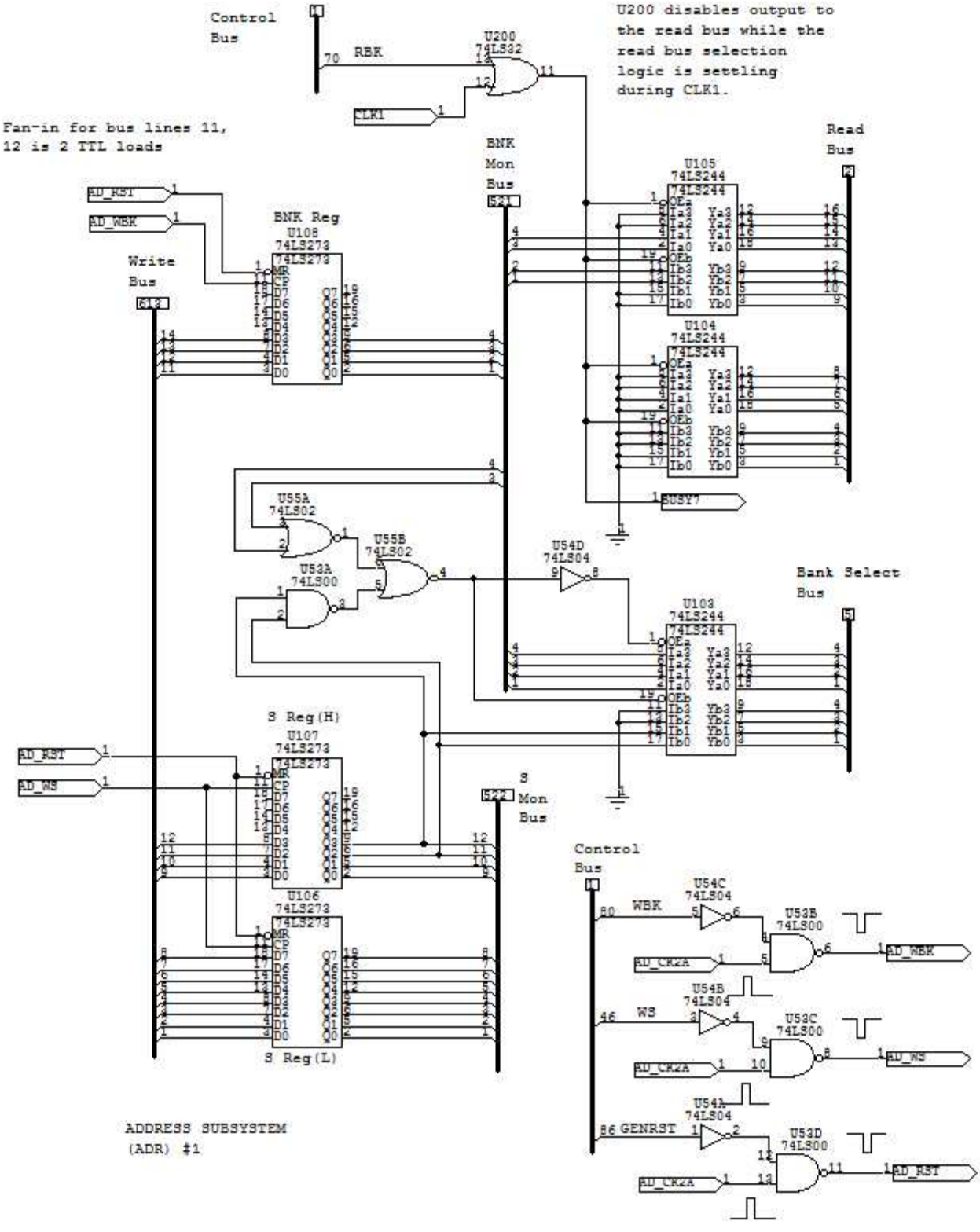
ADR INPUTS:

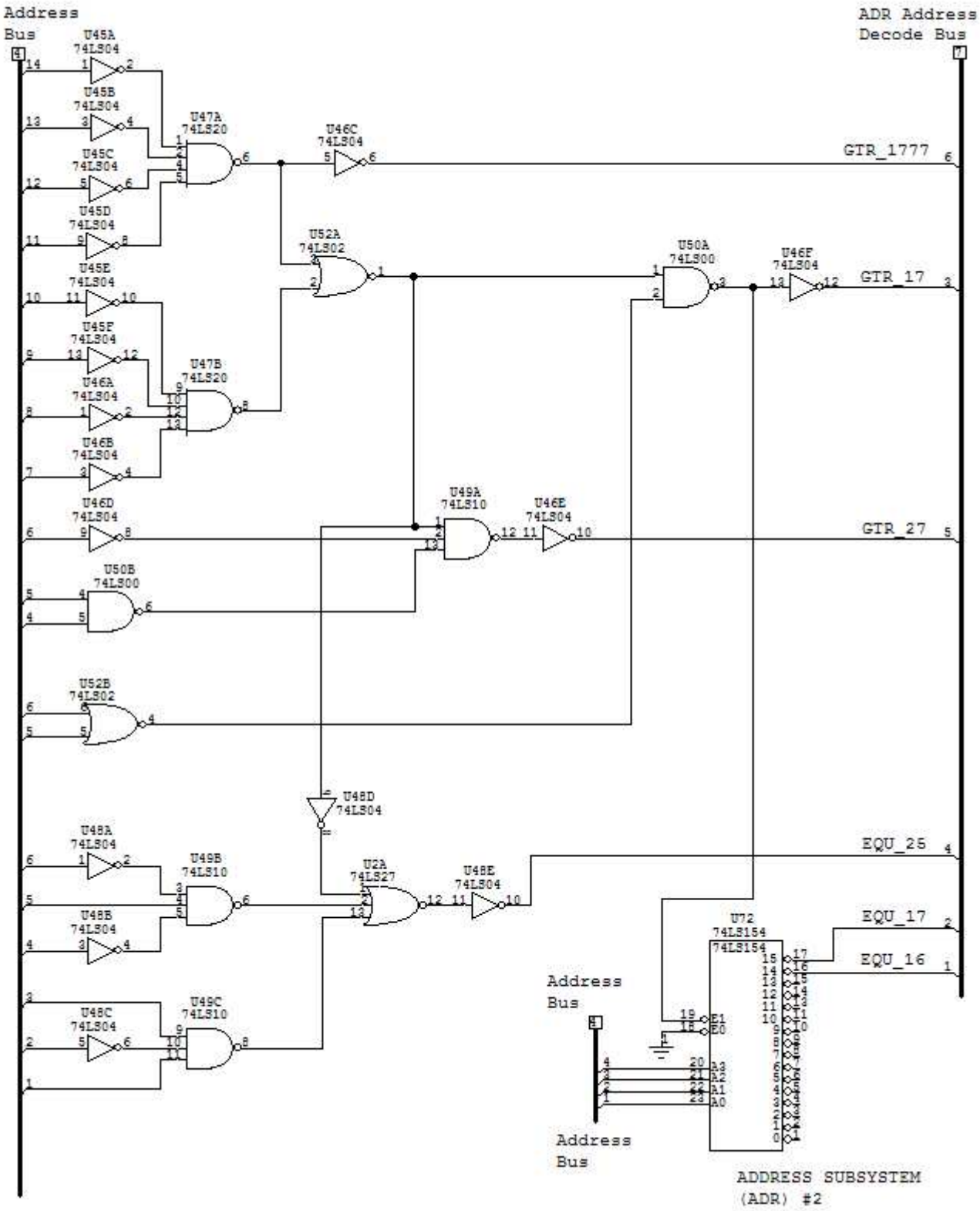
I/F	signal	full name	state definition
CLK:			
	CLK1	CLOCK 1	1=read bus setup; inhibit read bus output
	CLK2	CLOCK 2	data transfer occurs on falling edge
CPM:			
	GENRST	GENERAL RESET	0=reset ADR registers
	RBK	READ BANK	0=output BNK register to read bus
	WBK	WRITE BANK	0=write into BNK register
from write bus			
	WS	WRITE S	0=write into S register from write bus
WBUS:			
	WB_01	WRITE BUS 01	
	...		
	WB_14	WRITE BUS 14	

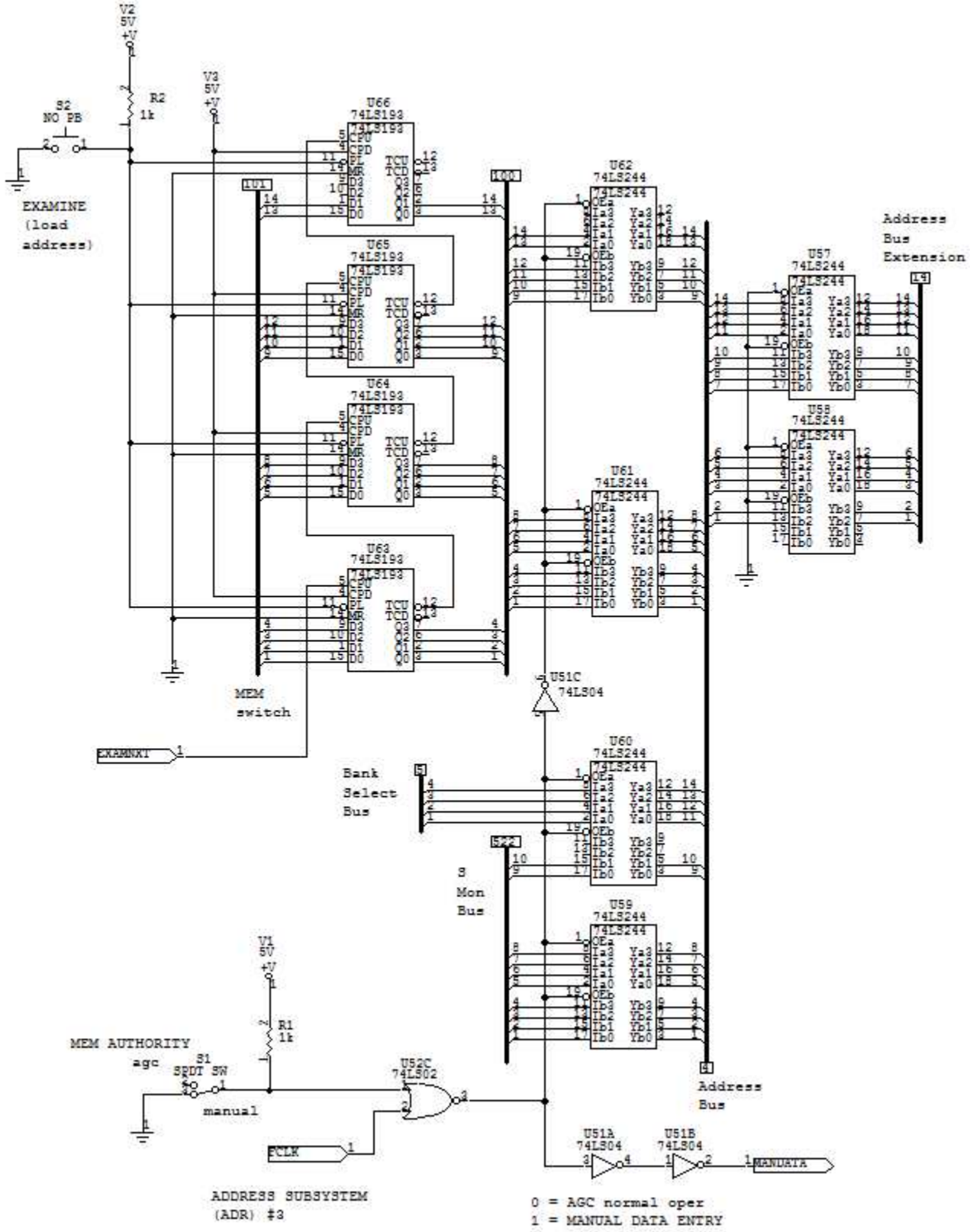


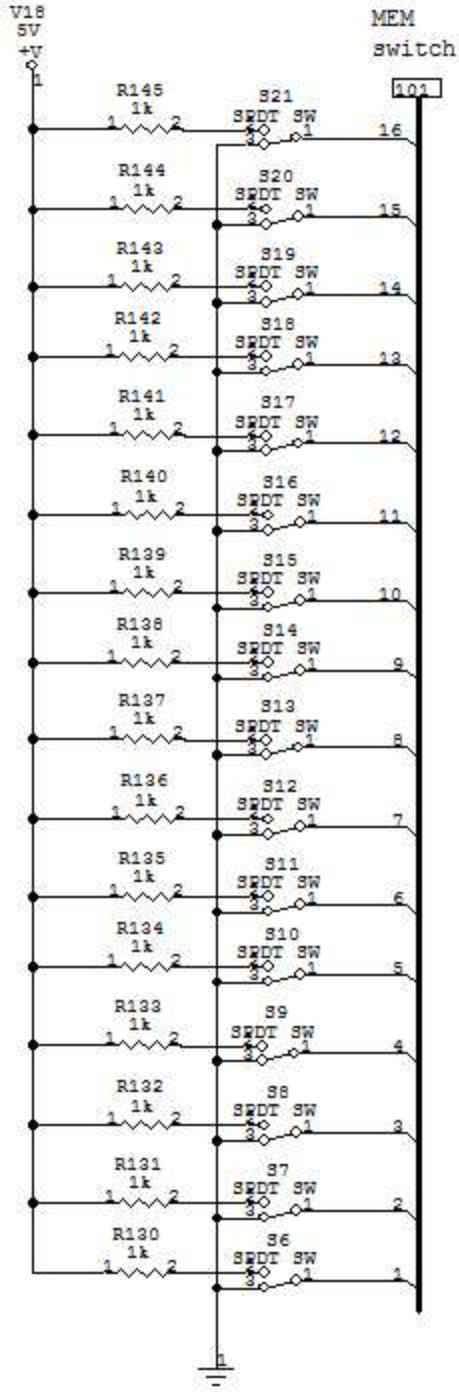
ADR OUTPUTS:

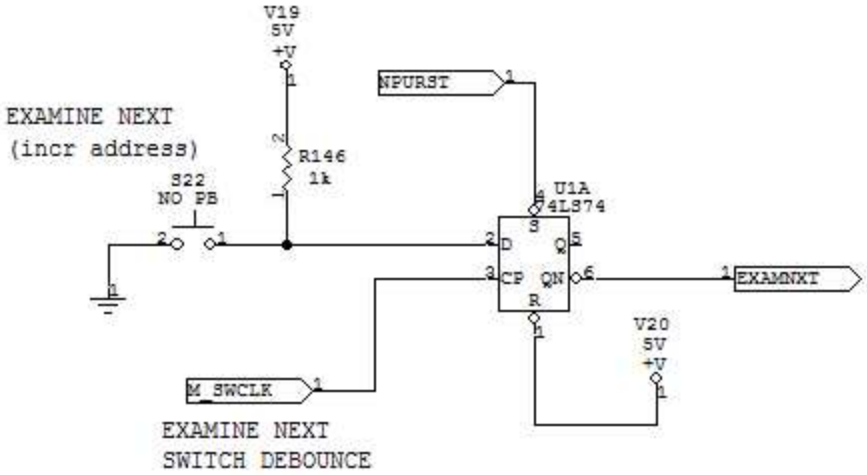
I/F	signal	full name	state definition
MEM:			
	AD_11	ADDRESS BUS 11	bank select bits
	...		
	AD_14	ADDRESS BUS 14	
	AD_1	ADDRESS BUS 1	low order address
	...		
	AD_10	ADDRESS BUS 10	
various:			
	EQU_16	ADDRESS = 016	0=CADR in reg S = 016
	EQU_17	ADDRESS = 017	0=CADR in reg S = 017
	GTR_17	ADDRESS > 017	0=CADR in reg S > 017
	EQU_25	ADDRESS = 025	0=CADR in reg S = 025
	GTR_27	ADDRESS > 027	0=CADR in reg S > 027
	GTR_1777	ADDRESS > 01777	0=CADR in reg S > 01777
RBUS:			
	RB_01	READ BUS 01	
	...		
	RB_16	READ BUS 16	
	BUSY	READ BUS BUSY	0=output to read bus

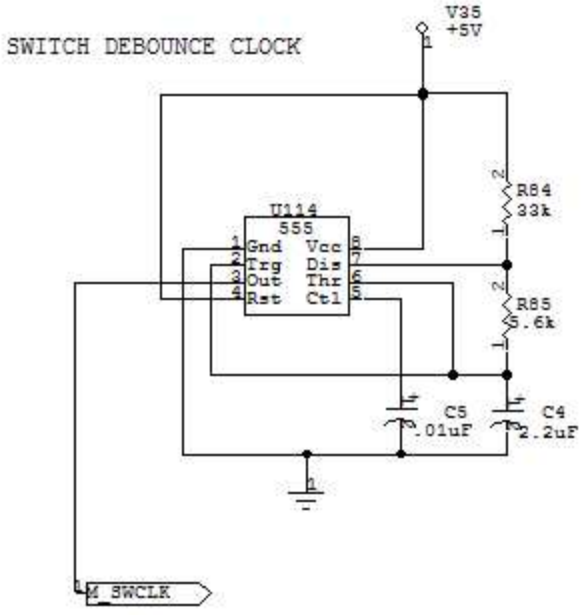

Control Bus
RBK
U200
74LS32
CLK1
U200 disables output to the read bus while the read bus selection logic is settling during CLK1.
Fan-in for bus lines 11, 12 is 2 TTL loads
BNK Mon Bus
Read Bus
U105
74LS244
U104
74LS244
BUSY7
AD_RST
AD_WBK
BNK Reg
U108
74LS273
Write Bus
U55A
74LS02
U55B
74LS02
U53A
74LS00
U54D
74LS04
Bank Select Bus
U103
74LS244
S Reg(H)
U107
74LS273
AD_RST
AD_WS
S Mon Bus
U106
74LS273
S Reg(L)
Control Bus
U54C
74LS04
WBK
U53B
74LS00
AD_CK2A
AD_WBK
U54B
74LS04
WS
U53C
74LS00
AD_WS
U54A
74LS04
GENRST
U53D
74LS00
AD_RST
ADDRESS SUBSYSTEM
(ADR) #1


Address
Bus
ADR Address
Decode Bus
U45A
74LS04
U45B
74LS04
U45C
74LS04
U45D
74LS04
U45E
74LS04
U45F
74LS04
U46A
74LS04
U46B
74LS04
U46D
74LS04
U47A
74LS20
U47B
74LS20
U46C
74LS04
U52A
74LS02
U50A
74LS00
U46F
74LS04
GTR_1777
GTR_17
U49A
74LS10
U46E
74LS04
GTR_27
U50B
74LS00
U52B
74LS02
U48D
74LS04
U48A
74LS04
U48B
74LS04
U48C
74LS04
U49B
74LS10
U49C
74LS10
U2A
74LS27
U48E
74LS04
EQU_25
U72
74LS154
EQU_17
EQU_16
Address
Bus
Address
Bus
ADDRESS SUBSYSTEM
(ADR) #2


V2
5V
+V
R2
1k
S2
NO PB
EXAMINE
(load
address)
V3
5V
+V
U66
74LS193
U65
74LS193
U64
74LS193
U63
74LS193
101
100
MEM
switch
EXAMNX1
U62
74LS244
U57
74LS244
U58
74LS244
U61
74LS244
Address
Bus
Extension
14
U51C
74LS04
U60
74LS244
Bank
Select
Bus
5
S
Mon
Bus
502
U59
74LS244
Address
Bus
6
V1
5V
+V
R1
1k
MEM AUTHORITY
agc
S1
SPDT SW
manual
U52C
74LS02
SCLK
U51A
74LS04
U51B
74LS04
MANUATA
ADDRESS SUBSYSTEM
(ADR) #3
0 = AGC normal oper
1 = MANUAL DATA ENTRY







ADDRESS SUBSYSTEM
(ADR) #4

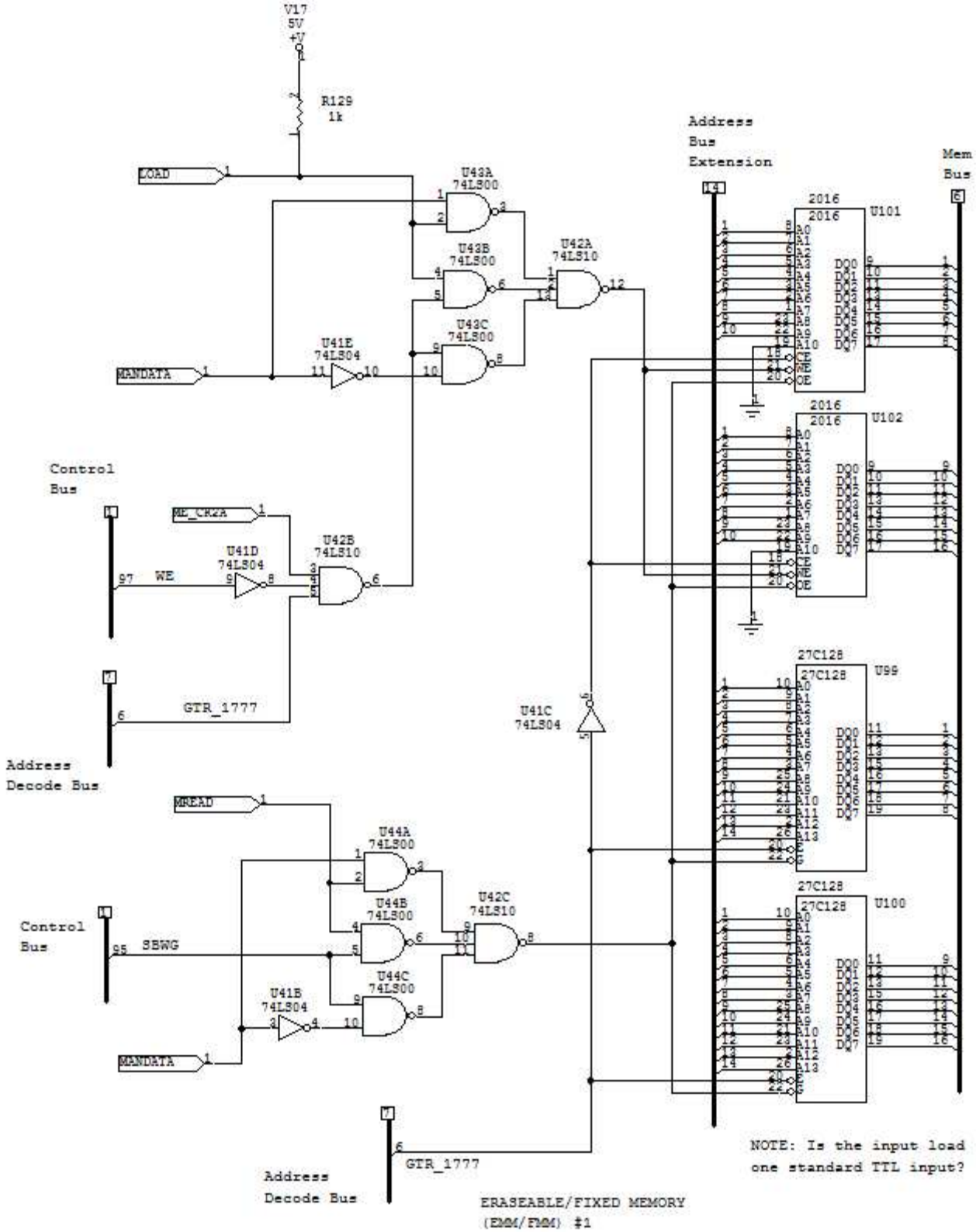
EMM/FMM (Eraseable/Fixed Memory)

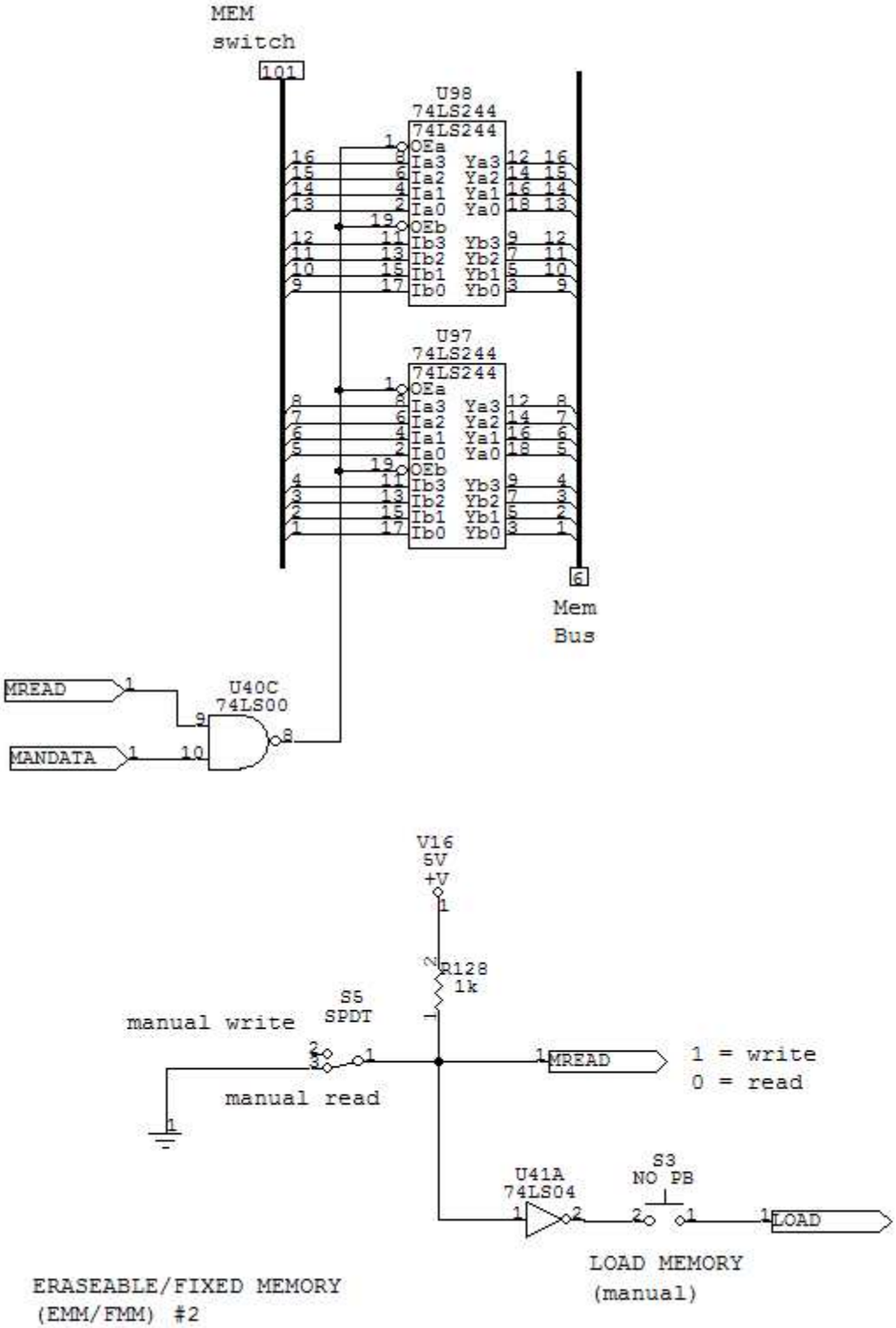
MEM INPUTS:

I/F	signal	full name	state definition
CLK:			
	CLK2	CLOCK 2	data transfer occurs on CLK2
CPM:			
	WE	WRITE ERASEABLE	0=write memory bus to eraseable memory
	SBWG	WRITE G (MEM)	0=read eraseable or fixed memory onto memory bus
ADR:	GTR_1777	ADDRESS > 01777	0=CADR in reg S > 01777
	AD_01	ADDRESS BUS 01	
	...		
	AD_10	ADDRESS BUS 10	
	AD_11	ADDRESS BUS 11	bank select portion of address bus
	...		
	AD_14	ADDRESS BUS 14	bank select portion of address bus

BIDIRECTIONAL (IN/OUT):

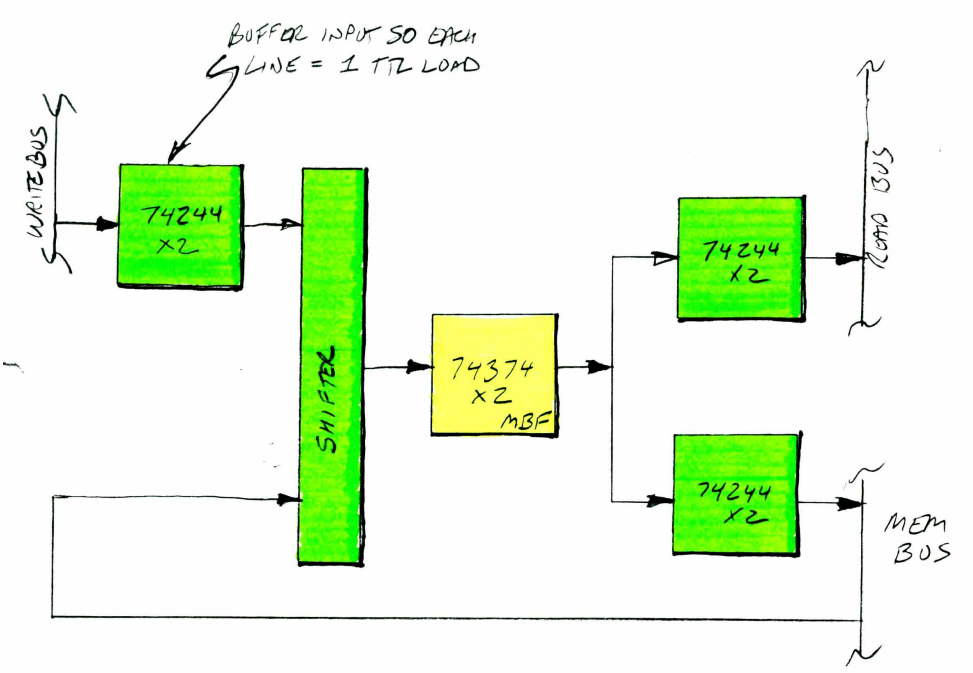
I/F	signal	full name	state definition
EMM/FMM:			
	MEM_01	MEMORY_BUS 01	Memory word formats:
	...		inst: 15-13:op code; 12-1:address
	MEM_15	MEMORY_BUS 15	data: 15:SG; 14-1 data
	MEM_16	MEMORY_BUS 16	parity (odd) bit for memory bus


V17
5V
+V
R129
1k
LOAD
MANDATA
U43A
74LS00
U43B
74LS00
U43C
74LS00
U42A
74LS10
U41E
74LS04
Address
Bus
Extension
Mem
Bus
2016
U101
2016
U102
27C128
U99
27C128
U100
Control
Bus
ME_CR2A
U41D
74LS04
U42B
74LS10
WE
GTR_1777
Address
Decode Bus
U41C
74LS04
MREAD
U44A
74LS00
U44B
74LS00
U44C
74LS00
U42C
74LS10
U41B
74LS04
SBWG
NOTE: Is the input load
one standard TTL input?
ERASEABLE/FIXED MEMORY
(EMM/FMM) #1



ERASEABLE/FIXED MEMORY
(EMM/FMM) #2

MBF (Memory Buffer Register)



The AGC has a 16-bit G register for transferring data to and from memory. WRITE bus data can be written directly into the G register, or can be bit-shifted before writing. Data from the G register can be copied to the READ bus, or to the memory bus.

The following section shows how bits are shifted in bus-to-register-to-memory transfers. The row of 16 comma-separated entries represent bit locations at the destination; the leftmost entry is the MSB, and the rightmost is the LSB. The designation in each location identifies source bit location. This will become clearer shortly.

In memory, the 16th bit is the odd parity bit, and the 15th bit is the sign. In the G register, the bits are flipped: the 16th bit is the sign, and the 15th bit is the parity. The WE pulse, which writes from the G register to memory, causes the sign bit (SG; bit 16 in G) to be written to bit 15 in memory. Parity is written to memory from the parity generator (PAR), not from the parity bit in G. (The G parity bit holds the parity read from memory.)

WE:

BX, SG, B14, B13, B12, B11, B10, B9, B8, B7, B6, B5, B4, B3, B2, B1

Data is written from memory to G by the SBWG control pulse. The sign in memory (SG; bit 15) is written to bit 16 in G. The parity bit (bit 16 in memory) is written to bit 15 in G by the PAR subsystem.

SBWG:

SG, BX, B14, B13, B12, B11, B10, B9, B8, B7, B6, B5, B4, B3, B2, B1

Data is written into G from the WRITE bus using WG (no shift), or one of the following control pulses that produce the following shifts:

W20:

B1, BX, SG, B14, B13, B12, B11, B10, B9, B8, B7, B6, B5, B4, B3, B2

W21:

SG, BX, SG, B14, B13, B12, B11, B10, B9, B8, B7, B6, B5, B4, B3, B2

W22:

B14, BX, B13, B12, B11, B10, B9, B8, B7, B6, B5, B4, B3, B2, B1, SG

W23:

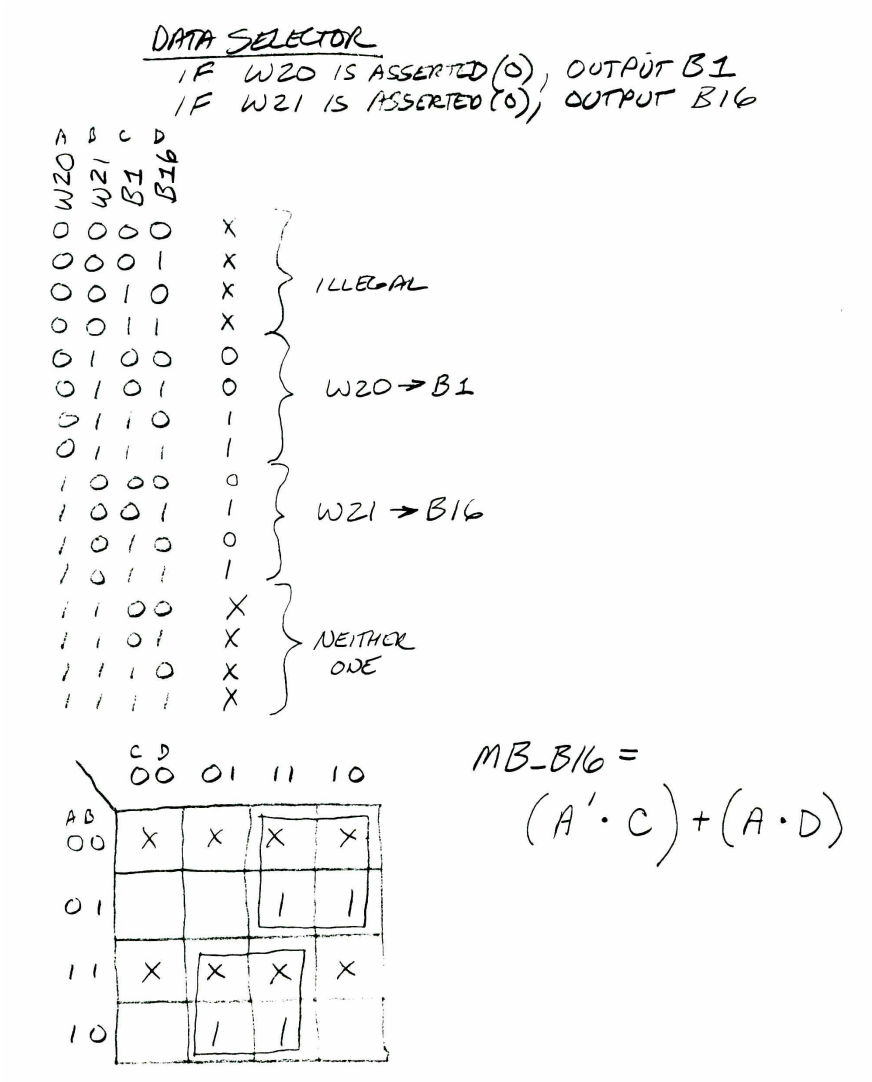
SG, BX, B13, B12, B11, B10, B9, B8, B7, B6, B5, B4, B3, B2, B1, SG

Data is read from G to the READ bus as follows. The parity bit (bit 15 in G) is not transferred to the read bus; instead, the sign bit is copied onto bits 15 and 16 of the READ bus.

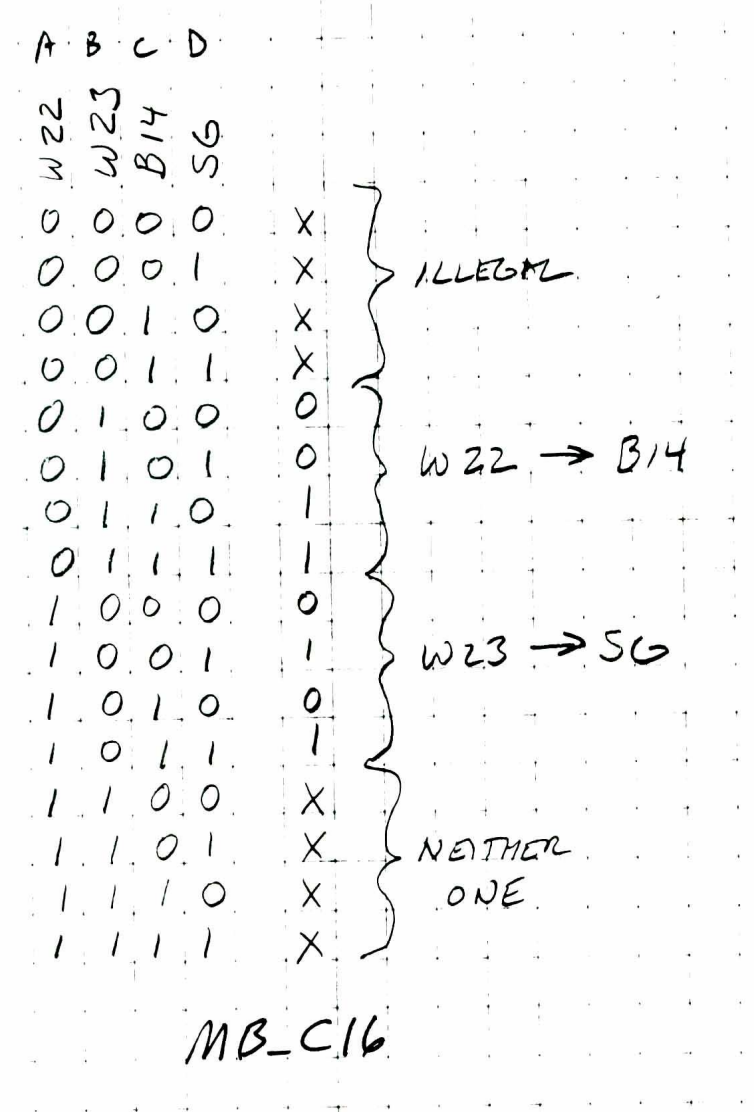
RG:

SG, SG, B14, B13, B12, B11, B10, B9, B8, B7, B6, B5, B4, B3, B2, B1

Some of the design that went into the combinational logic that sets bit 16 in the G register from the READ bus is shown here. The MB_B16 output controls the 16th bit for the W20 and W21 control pulses.

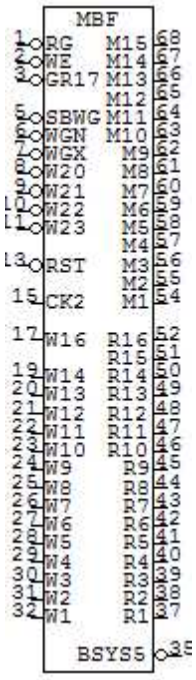


The MB_C16 output controls the 16th bit for the W22 and W23 control pulses.



MBF INPUTS:

I/F	signal	full name	state definition
CLK:			
	CLK1	CLOCK 1	1=read bus setup; inhibit read bus output
	CLK2	CLOCK 2	data transfer occurs on falling edge
CPM:			
	RG	READ G	0=output G register to read/write bus
	WE	WRITE ERASEABLE	0=output G register to memory bus
	GTR_17	ADDRESS > 017	0=CADR in register S > 017
	SBWG	WRITE G (MEM)	0=write G from memory bus
	WGN	WRITE G	0=write G from read/write bus (no shift)
	WGX	WRITE G	0=write G from read/write bus (no shift)
	W20	WRITE G (SHIFT)	0=write G
	W21	WRITE G (SHIFT)	0=write G
	W22	WRITE G (SHIFT)	0=write G
	W23	WRITE G (SHIFT)	0=write G
	GENRST	GENERAL RESET	0=General Reset
WBUS:			
	WB_01	WRITE BUS 01	
	...		
	WB_14	WRITE BUS 14	
	WB_15	WRITE BUS 15	US (overflow) bit for write bus
	WB_16	WRITE BUS 16	SG (sign) bit for write bus

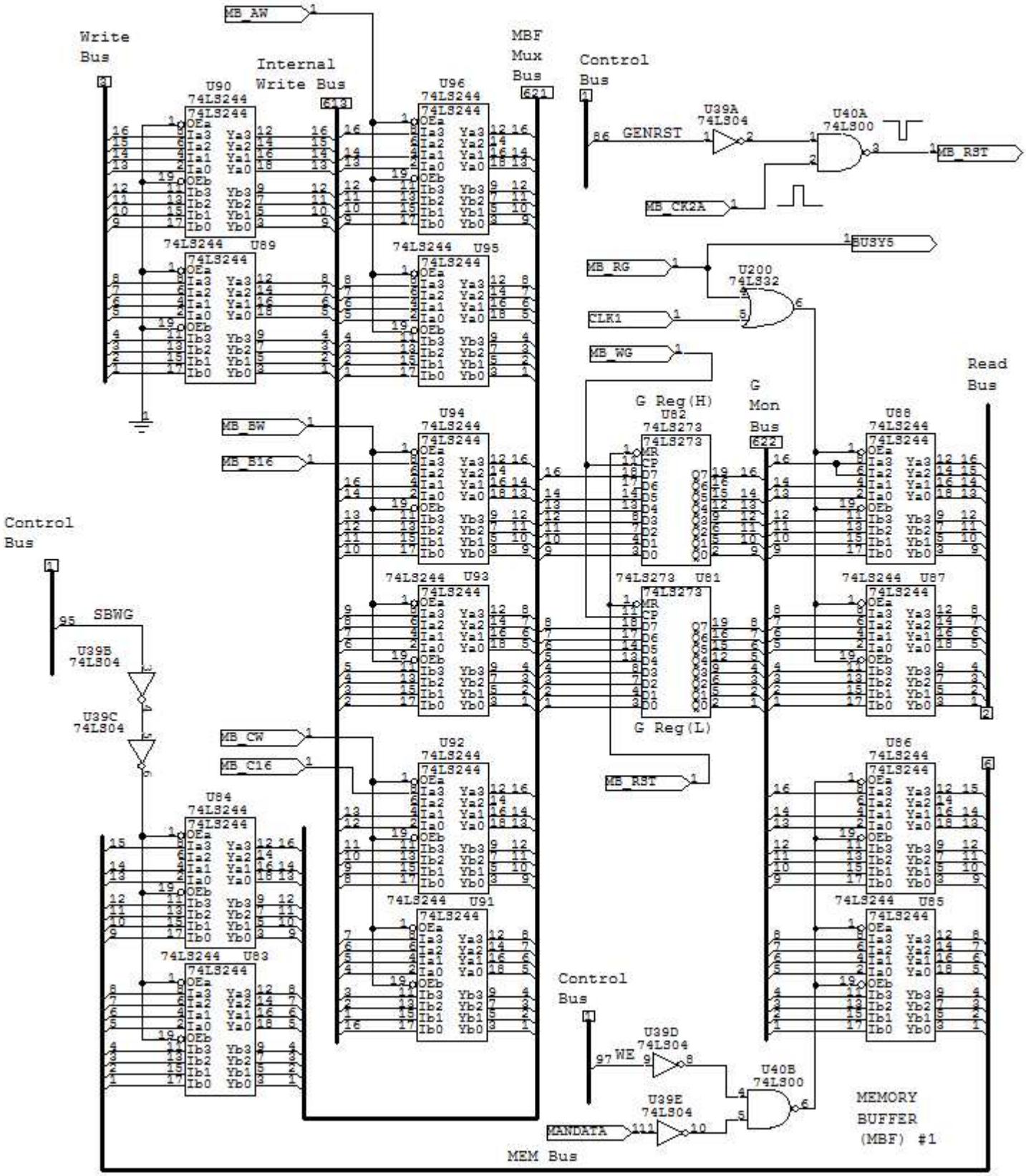


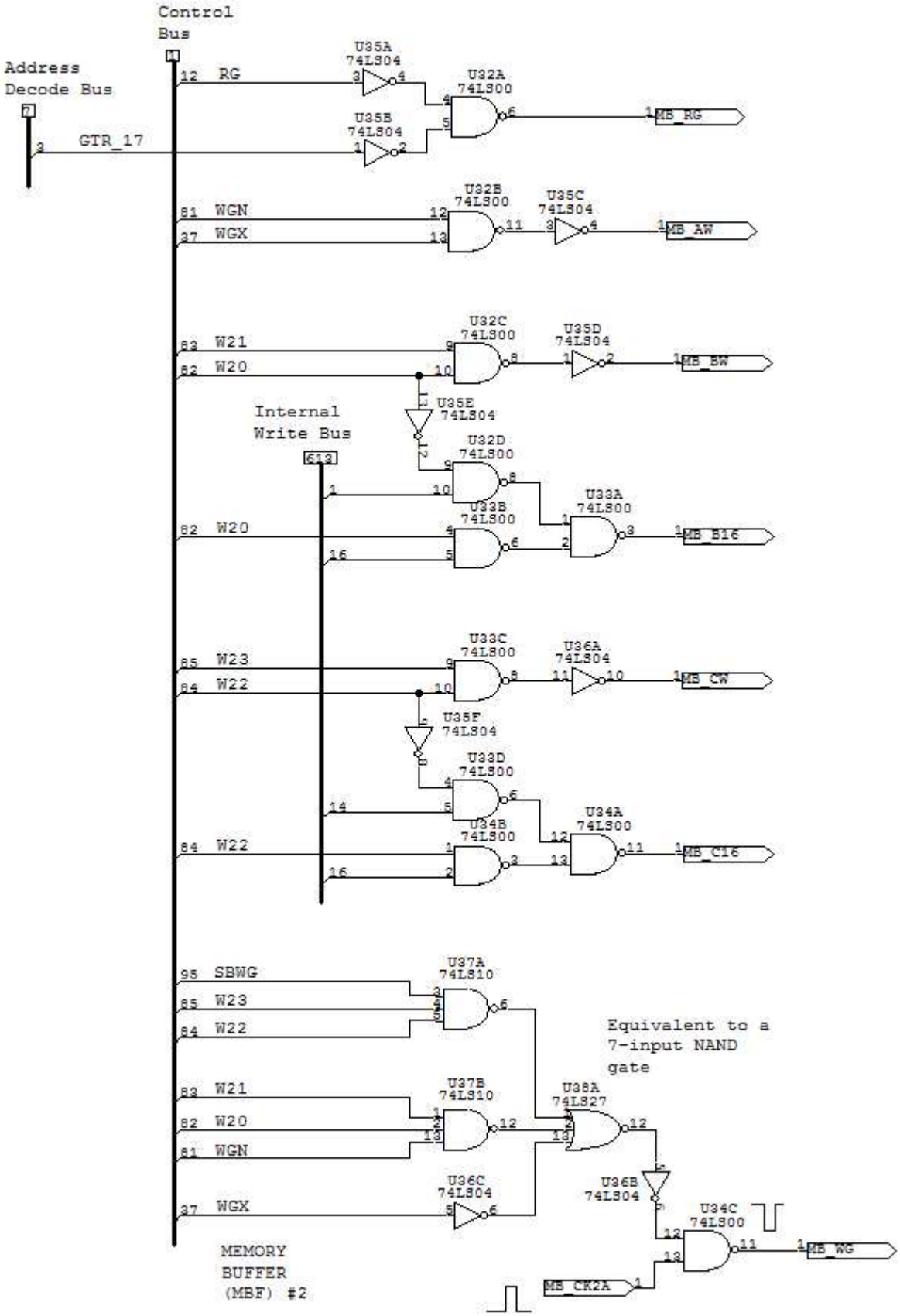
MBF OUTPUTS:

I/F	signal	full name	state definition
RBUS:			
	RB_01	READ BUS 01	
	...		
	RB_14	READ BUS 14	
	RB_15	READ BUS 15	US (overflow) bit for read/write bus
	RB_16	READ BUS 16	SG (sign) bit for read/write bus
	BUSY	READ BUS BUSY	0=output enabled to read bus

BIDIRECTIONAL (IN/OUT):

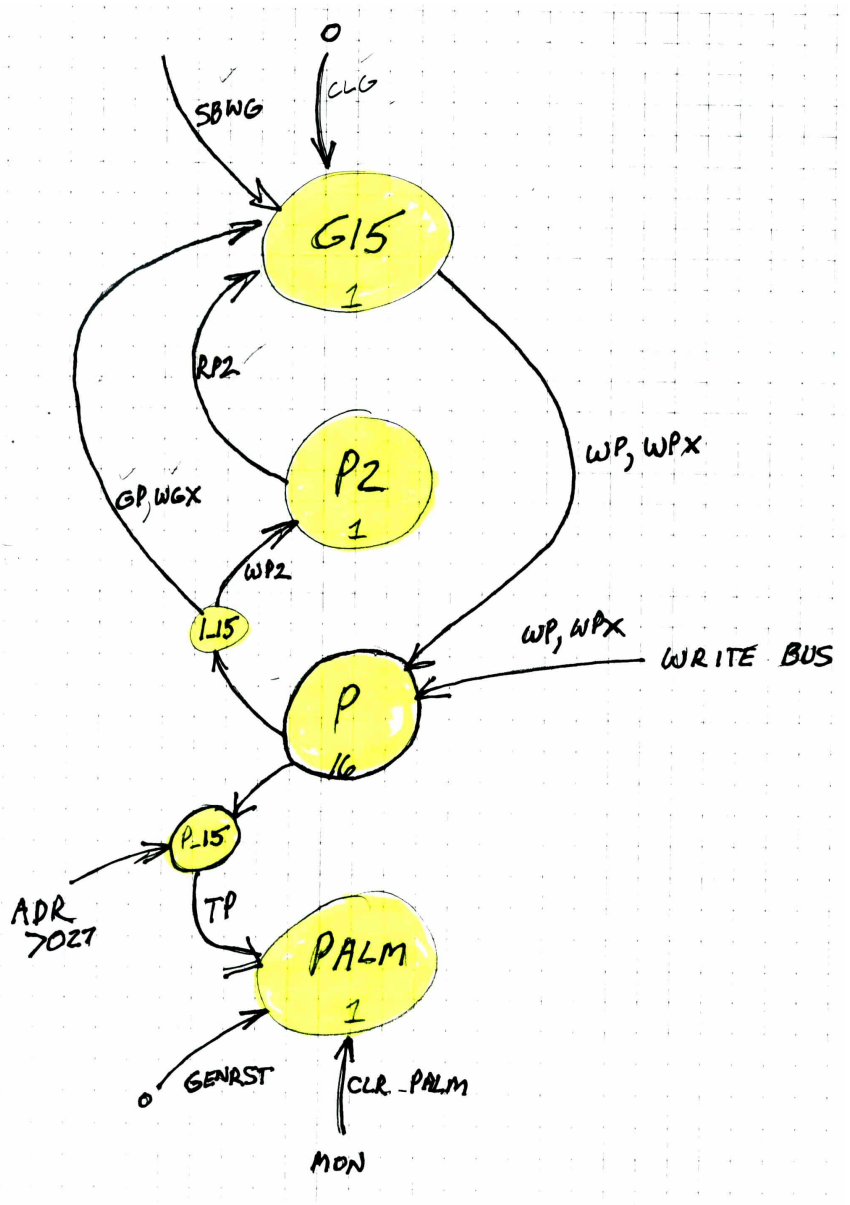
I/F	signal	full name	state definition
EMM/FMM:			
	MEM_01	MEMORY_BUS 01	Memory word formats:
	...		inst: 15-13:op code; 12-1:address
	MEM_15	MEMORY_BUS 15	data: 15:SG; 14-1 data
	MEM_16	MEMORY_BUS 16	parity (odd) bit for memory bus


Write Bus
Internal Write Bus
MBF Mux Bus
Control Bus
Read Bus
G Mon Bus
MB_AW
MB_BW
MB_B16
MB_CW
MB_C16
MB_WG
MB_RST
MB_CK2A
MB_RG
CLK1
GENRST
SBWG
WE
MANDATA
BUSY5
G Reg(H)
G Reg(L)
MEM Bus
MEMORY BUFFER (MBF) #1
U90 74LS244
U89 74LS244
U96 74LS244
U95 74LS244
U94 74LS244
U93 74LS244
U92 74LS244
U91 74LS244
U84 74LS244
U83 74LS244
U88 74LS244
U87 74LS244
U86 74LS244
U85 74LS244
U82 74LS273
U81 74LS273
U39A 74LS04
U39B 74LS04
U39C 74LS04
U39D 74LS04
U39E 74LS04
U40A 74LS00
U40B 74LS00
U200 74LS32

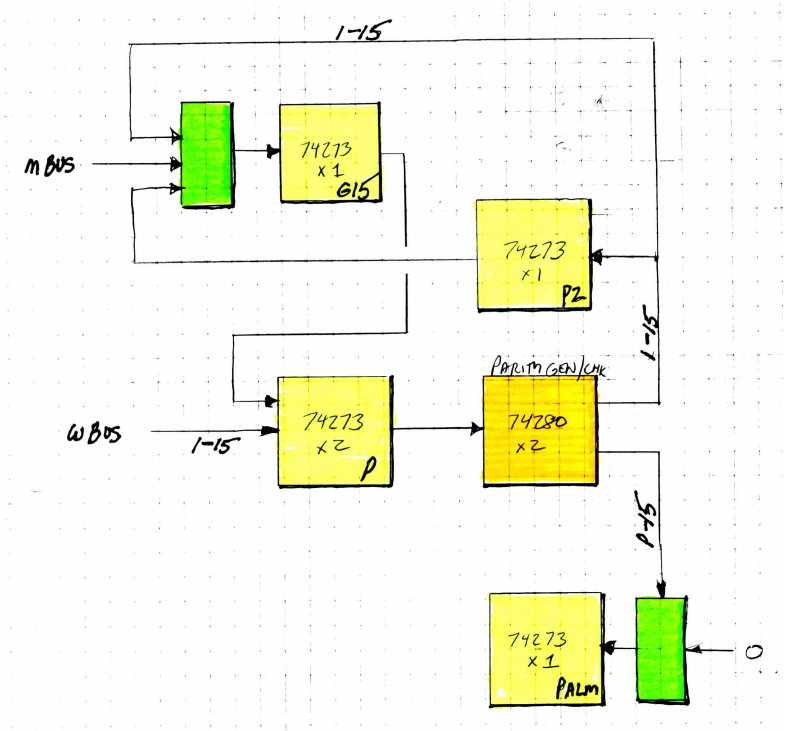

Control
Bus
Address
Decode Bus
7
3
GTR_17
12
RG
U35A
74LS04
U35B
74LS04
U32A
74LS00
MB_RG
81
WGN
87
WGX
U32B
74LS00
U35C
74LS04
MB_AW
83
W21
82
W20
U32C
74LS00
U35D
74LS04
MB_BW
U35E
74LS04
Internal
Write Bus
613
U32D
74LS00
U33A
74LS00
U33B
74LS00
MB_B16
16
85
W23
84
W22
U33C
74LS00
U36A
74LS04
MB_CW
U35F
74LS04
U33D
74LS00
14
U34A
74LS00
U34B
74LS00
MB_C16
95
SBWG
U37A
74LS10
Equivalent to a
7-input NAND
gate
U37B
74LS10
U38A
74LS27
U36C
74LS04
U36B
74LS04
U34C
74LS00
MB_WG
MB_CK2A
MEMORY
BUFFER
(MBF) #2

PAR (Parity Generation and Test)

The PAR subsystem checks the memory parity bit during each memory cycle and generates an alarm if the parity bit in memory does not match the expected odd parity. The PAR subsystem also generates parity from the contents of G and writes this parity back to memory.

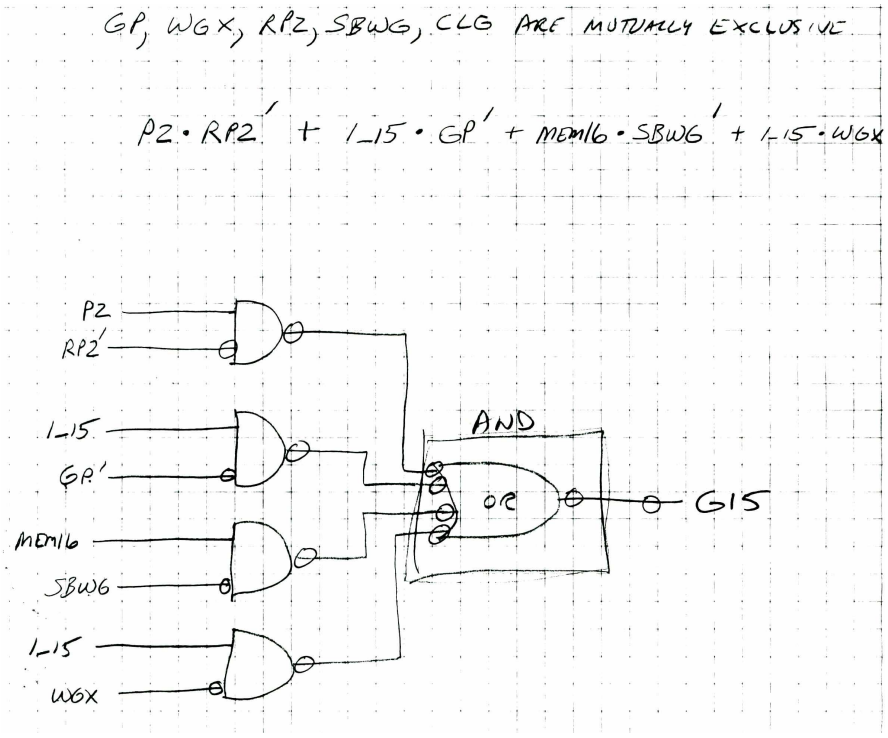


This block diagram of the PAR subsystem emerges from the previous diagram.



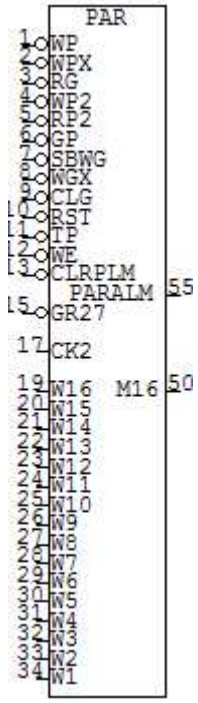
This is the combinational logic used to generate the input to the G15 register. This is the 1-bit register that holds bit 15 (the parity bit) for the G register. The remainder of the G register (bits 1-14 and bit 16) is in the MBF subsystem.

The minterms are written out on top. DeMorgan's Theorem and a little bubble-pushing changes the OR gate into a NAND.



PAR INPUTS:

I/F	signal	full name	state definition
CLK:			
	CLK2	CLOCK 2	data transfer occurs on falling edge
CPM:			
	RG	READ G15	0=write G15 into P
	RP2	READ P2	0=write P2 into G15
	WP	WRITE P	0=write P (same as WPX)
	WPX	WRITE P	0=write P (same as WP)
	WP2	WRITE P2	0=write P2 from 1-15 generator
	SBWG	WRITE G15 (MEM)	0=write G15 from memory parity bit
	GP	WRITE G15	0=write G15 from 1-15 generator (same as WGX)
	WGX	WRITE G15	0=write G15 from 1-15 generator (same as GP)
	CLG	CLEAR G15	0=clear G15
	TP	TEST PARITY	0=test parity from P-15
ADR:			
	GTR_27	ADDRESS > 027	0=CADR in Register S evaluates to > 027
WBUS:			
	WB_01	WRITE BUS 01	
	...		
	WB_14	WRITE BUS 14	
	WB_15	WRITE BUS 15	US (overflow) bit for write bus
	WB_16	WRITE BUS 16	SG (sign) bit for write bus
MON:			
	CLRPLM	CLEAR PARITY ALM	0=clear parity alarm

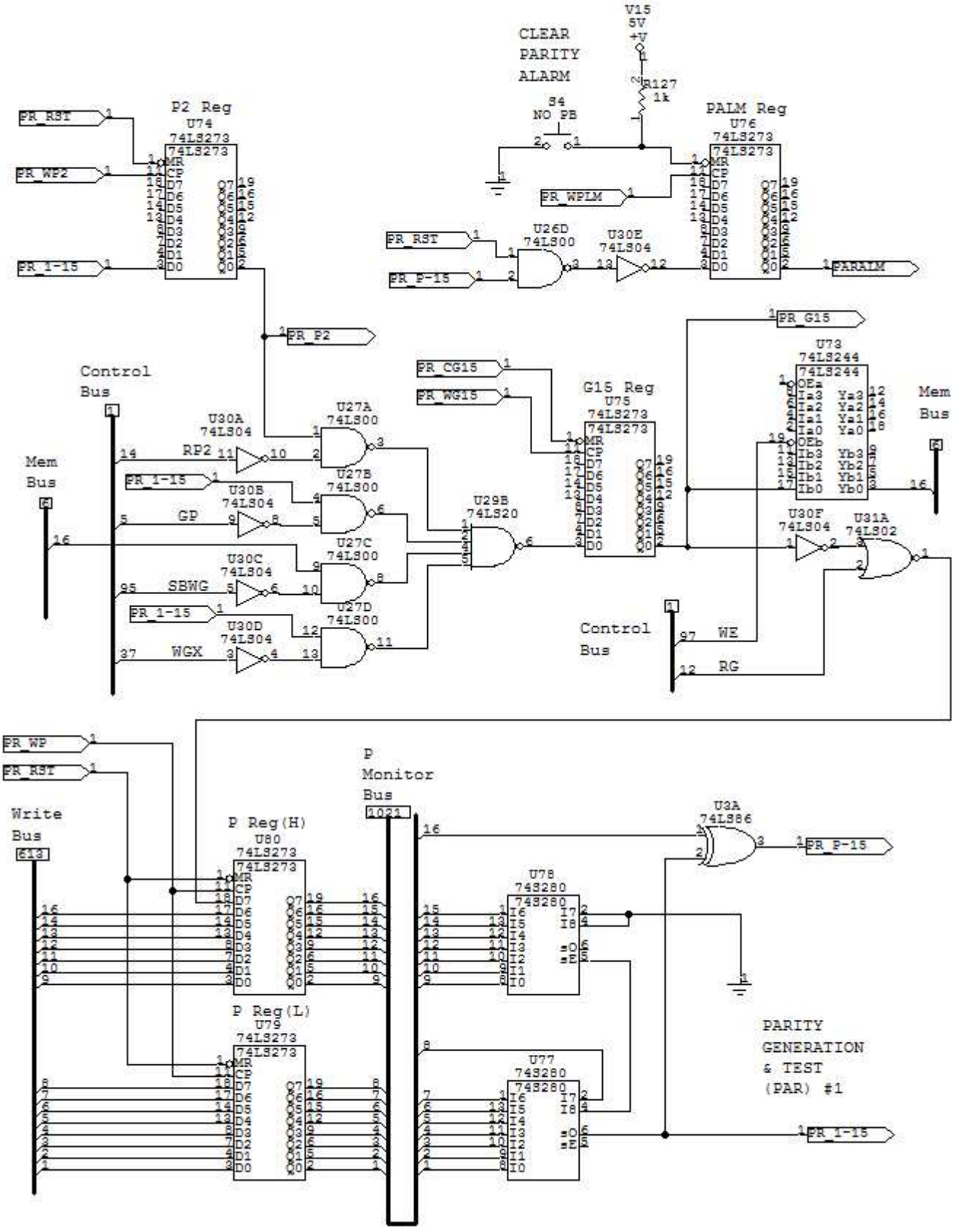


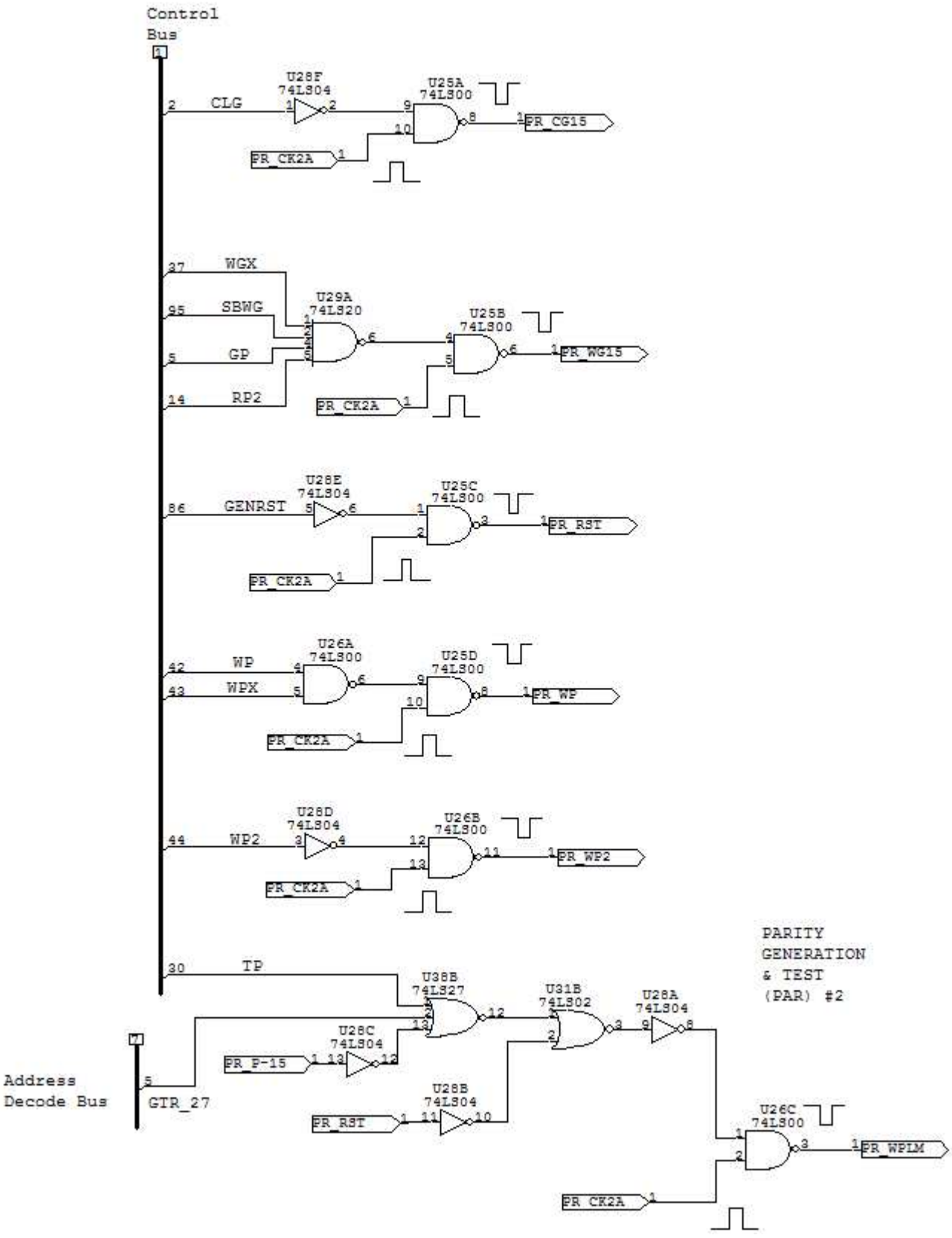
PAR OUTPUTS:

I/F	signal	full name	state definition
MON			
	PARALM	PARITY ALARM	1=parity alarm

BIDIRECTIONAL (IN/OUT):

I/F	signal	full name	state definition
EMM/FMM:			
	MEM_16	MEMORY_BUS 16	parity (odd) bit for memory bus

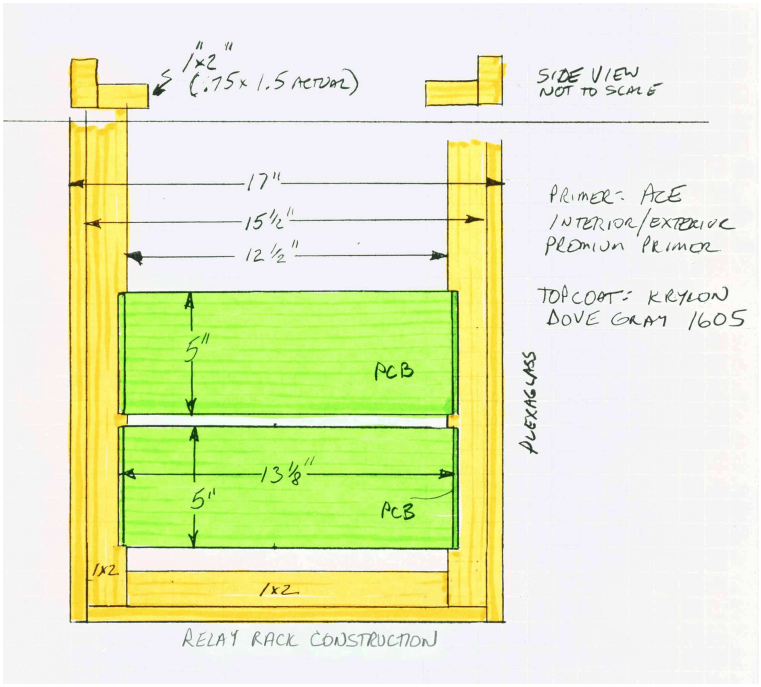

CLEAR
PARITY
ALARM
V15
5V
+V
R127
1k
S4
NO PB
P2 Reg
U74
74LS273
PALM Reg
U76
74LS273
PR_RST
PR_WP2
PR_1-15
PR_WPLM
U26D
74LS00
U30E
74LS04
PR_P-15
PARALM
PR_P2
PR_G15
U73
74LS244
Control
Bus
Mem
Bus
U30A
74LS04
U27A
74LS00
U27B
74LS00
U30B
74LS04
U27C
74LS00
U30C
74LS04
U27D
74LS00
U30D
74LS04
RP2
GP
SBWG
WGX
PR_CG15
PR_WG15
G15 Reg
U75
74LS273
U29B
74LS20
U30F
74LS04
U31A
74LS02
WE
RG
PR_WP
Write
Bus
613
P
Monitor
Bus
1021
P Reg(H)
U80
74LS273
P Reg(L)
U79
74LS273
U78
74S280
U77
74S280
U3A
74LS86
PARITY
GENERATION
& TEST
(PAR) #1


Control
Bus
U28F
74LS04
U25A
74LS00
2
CLG
1
2
9
10
8
1
PR_CG15
PR_CK2A
1
37
WGX
95
SBWG
5
GP
14
RP2
U29A
74LS20
U25B
74LS00
6
4
5
6
1
PR_WG15
PR_CK2A
1
U28E
74LS04
U25C
74LS00
86
GENRST
5
6
1
2
3
1
PR_RST
PR_CK2A
1
U26A
74LS00
U25D
74LS00
42
WP
43
WPX
4
5
6
9
10
8
1
PR_WP
PR_CK2A
1
U28D
74LS04
U26B
74LS00
44
WP2
3
4
12
13
11
1
PR_WP2
PR_CK2A
1
PARITY
GENERATION
& TEST
(PAR) #2
30
TP
U38B
74LS27
U31B
74LS02
U28A
74LS04
U26C
74LS00
7
Address
Decode Bus
5
GTR_27
U28C
74LS04
PR_P-15
1
13
12
U28B
74LS04
PR_RST
1
11
10
1
2
3
1
PR_WPLM
PR_CK2A
1

Fabrication

The MEM module is (3) 13"x5" circuit boards, and 1 control panel.

Module Rack



The module framework is designed to resemble a relay rack, but scaled to fit the circuit board dimensions. It is constructed out of 1"x2" pine and spray-painted semi-gloss gray.

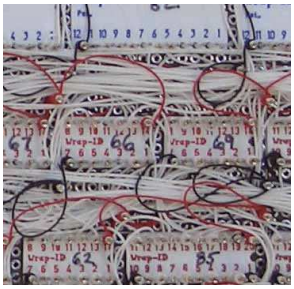
Circuit boards are mounted to the rack by 2 phillips screws at either end. Nylon spacers (1/4") are used as standoffs to hold the board edges above the rack. The boards are mounted so the chips are in the back and the pins are wiring are visible from the front.

Power is distributed by 2 heavy aluminum bus bars mounted vertically, one per side, on the back of the module. Machine screws are mounted through the bus bars at evenly-spaced intervals to provide connection points for the boards.

Solid copper wire (24 gauge) connects the boards to the bus bars. Ring terminals are used on the bus bar side of the connection. On the circuit board size, the wires are soldered directly to the supply rails.

Materials were purchased from Home Depot, ACE Hardware, and Radio Shack.

Circuit Boards



The circuit boards are 13"x5" general purpose prototyping boards, epoxy glass with double-side plated through pads on 0.1" centers (JAMECO 21477CL).

ICs are mounted in level 3 machine tooled wire-wrap sockets: 8, 14, 16, 20, 24, and 28 pin (JAMECO). Each socket has the pin-out labeled with a wire-wrap socket ID marker, which slips onto the socket before wrapping (JAMECO). The part number is written onto the ID marker.

Sockets are arranged in 4 horizontal rows on each board, with about 10 sockets per row.

Power is distributed on the back-side of each board by bare 24-gauge solid copper wire supply rails soldered at equal intervals to Klipwrap terminals: 3-prong terminals with a square tail for wire-wrapping (JAMECO 34163CL). A +5V rail runs above each row of sockets

and a ground rail runs below. Each rail connects directly to the aluminum module power bus using a ring tail connector.

On the pin side of the board, all connections are made with 30 AWG Kynar wire-wrap wire (JAMECO). Red wire is used for direct connections to the +5V supply rail. Black wire is used for direct connections to ground. White wire is used for everything else.

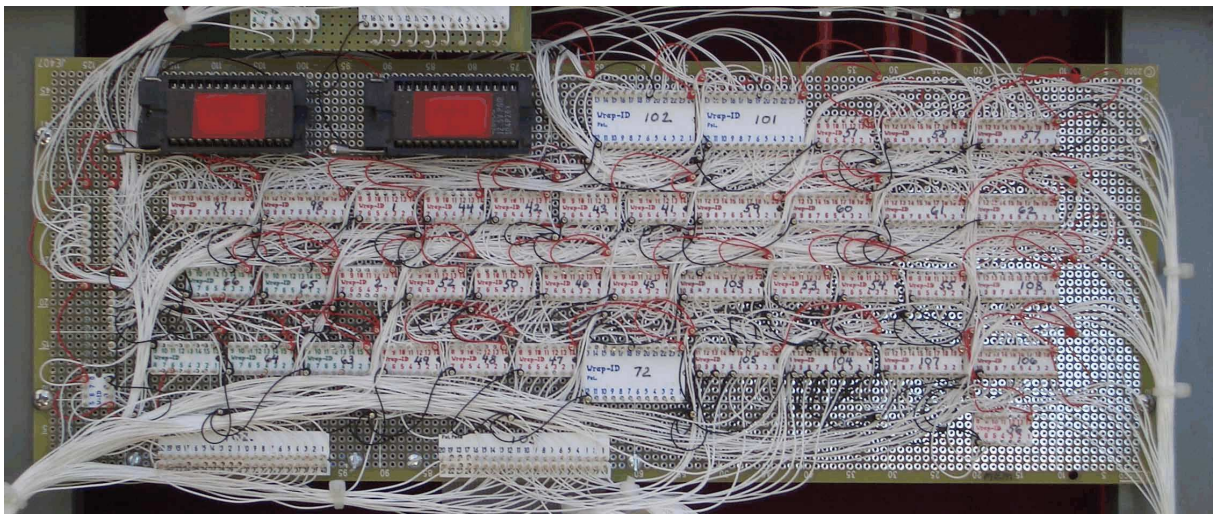
Power connections from the supply rails to each ICs are double-wrapped. Bypassing capacitors (.1 uf disc) are soldered across the supply rails at the Klipwrap terminals; about 1 capacitor for every 2 IC packages.

All connections were stripped and hand-wrapped using a Radio Shack hand-wrap tool. As each connection was made, the corresponding line on the schematic was marked with a colored highlighter.

DIP resistor networks (JAMECO) plugged into 20-pin wire-wrap sockets were used as current limiting resistors for the panel indicators.

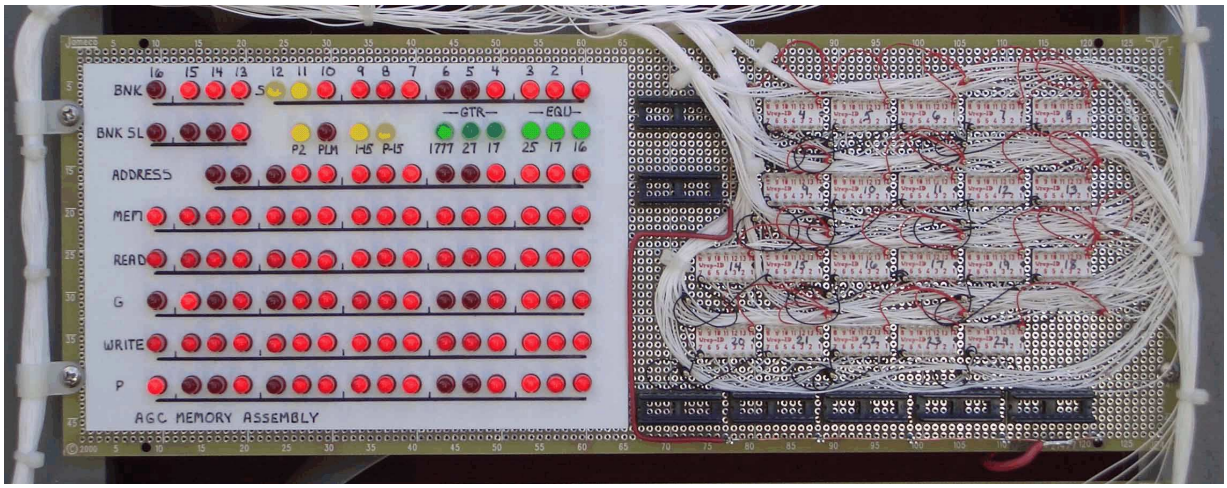
MEM Printed Circuit Board (PCB) A

The A board contains the zero-insertion force (ZIF) sockets for the fixed memory EPROMs, and the 2 40-pin IDE connectors that interface to the other modules. The eraseable memories (U101, U102) are also clearly visible next to the EPROMs. The Memory Address (ADR) and Eraseable/Fixed Memory (EMM/FMM) subsystems are primarily located on this board.



MEM Printed Circuit Board (PCB) B

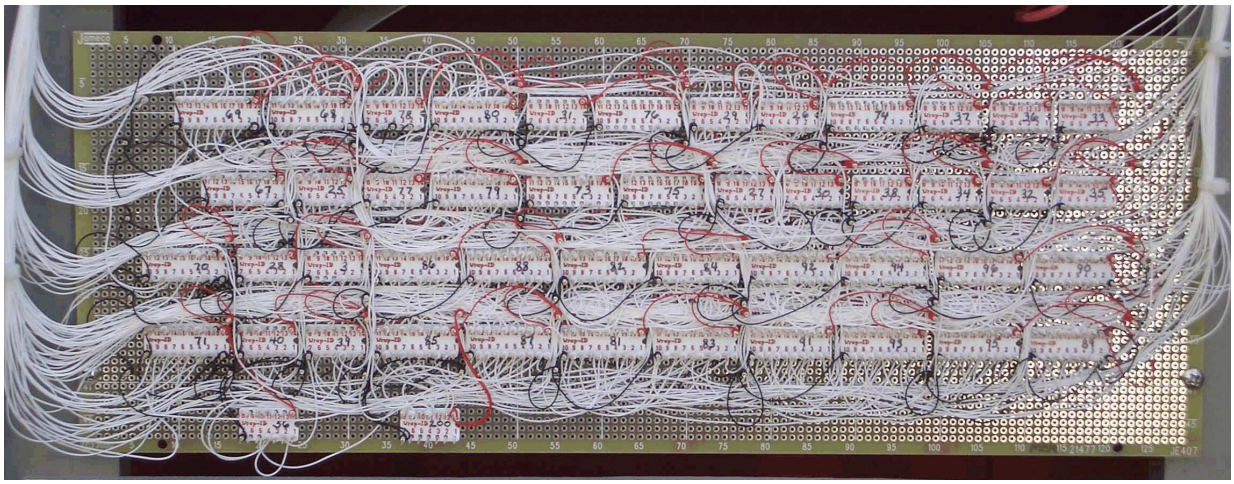
The B board contains the display indicators, their current-limiting resistor networks, and the open collector drivers. The display panel is a sheet of white styrene plastic. A push pin was used to make holes through the plastic and the LEDs were inserted in rows. The panel was



hand-lettered with an indelible marker.

MEM Printed Circuit Board (PCB) C

The C board primarily contains the Memory Buffer (MBF) and Parity Generation and Test (PAR) subsystems.



Parts (ICs)

74LS00	(11)	U50,U25,U26,U27,U40,U32,U33,U34,U43,U44,U53
74LS02	(3)	U52,U31,U55
74LS04	(12)	U39,U28,U51,U56,U48,U46,U45,U41,U30,U35,U36,U54
74LS06	(21)	U20,U19,U18,U15,U16,U17,U14,U13,U12,U10,U11,U9,U6,U7,U8,U5,U4,U21,U22,U23,U24
74LS10	(3)	U49,U37,U42
74LS20	(2)	U47,U29
74LS27	(2)	U2,U38
74LS74	(1)	U1
74LS86	(1)	U3
74LS154	(1)	U72
74LS193	(4)	U63,U64,U65,U66
74LS244	(31)	U57,U58,U59,U60,U61,U62,U67,U68,U69,U70,U71,U73,U83,U84,U85,U86,U87,U88,U89,U90,U91,U92,U93,U94,U95,U96,U97,U98,U103,U104,U105
74LS273	(10)	U74,U75,U76,U79,U80,U81,U82,U106,U107,U108
74S280	(2)	U77,U78
27C128	(2)	U99,U100
2016	(2)	U101,U102

Power Budget

	qty	mA (ea)	mA (tot)
74LS00	11	2.4	26.4
74LS02	3	2.4	7.2
74LS04	12	3.6	43.2
74LS06	21	3.6	75.6
74LS10	3	1.8	5.4
74LS20	2	1.2	2.4
74LS27	2	3.4	6.8
74LS74	1	4.0	4.0
74LS86	1	6.1	6.1
74LS154	1	6.2	6.2
74LS193	4	19.0	76.0
74LS244	31	32.0	992.0
74LS273	10	17.0	170.0
74LS280	2	16.0	32.0
27C128	2	25.0	50.0
2016	2	25.0	50.0
LED	124	20.0	2480.0

			4.0 Amps total
			1.6 Amps (excluding LEDs)